UNCLASSIFIED

AD 284 625

Reproduced
by the

ARMED SERVICES TECHNICAL INFORMATION AGENCY
ARLINGTON HALL STATION
ARLINGTON 12, VIRGINIA

UNCLASSIFIED

NOTICE: When government or other drawings, specifications or other data are used for any purpose other than in connection with a definitely related government procurement operation, the U. S. Government thereby incurs no responsibility, nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use or sell any patented invention that may in any way be related thereto.

AD NO. 284625
ASTIA FILE COPY
284625

SOLID STATE MICROELECTRONIC SYSTEMS PROGRAM

Final Report

Covering the Period
1 July 1961 to 31 June 1962

SC Contract No. DA-36-039-sc-87466

U. S. Army Signal Corps
Research and Development Laboratory
Fort Monmouth, New Jersey

GENERAL ELECTRIC COMPANY
HEAVY MILITARY ELECTRONICS DEPARTMENT
SYRACUSE, NEW YORK

Best Available Copy

$16.00

250p.

AD_____Accession No._____ UNCLASSIFIED

General Electric Company
Electronics Laboratory, Syracuse, New York

Solid State Microelectronic Systems Program

R. Warr, L. Ragonese, G. Danielson

1. Solid State Microelectronic Systems Program
2. Signal Corps Contract DA-36-039-sc-87466

Final Report
1 July 1961 to 30 June 1962
(238 pages incl. illus., tables)

Signal Corps Contract DA-36-039-sc-87466
Unclassified Report

A number of investigations have been carried out to assess the merits and limitations of the various forms of microelectronic circuitry. Specific tasks have been conducted to provide design criteria and information with the objective of improving microelectronic design and evaluation procedures. Solutions are given to the problem of how to design minimum power dissipation circuits. The effects of power dissipation, circuit tolerance, component tolerance and temperature on circuit reliability are considered. Solutions to the problem of attaining maximum circuit reliability are presented. It is shown how to evaluate various forms of microelectronic circuitry when only a limited number of terminals are available. The results of studies in the area of adjustability are presented.

Best Available Copy

SOLID STATE MICROELECTRONIC SYSTEMS PROGRAM

Final Report

Covering the Period

1 July 1961 to 30 June 1962

SC Contract No. DA-36-039-sc-87466

Placed by

U.S. Army Signal Corps
Research and Development Laboratory
Fort Monmouth, New Jersey

Prepared by

R. Warr
L. Ragonese
G. Danielson

GENERAL ELECTRIC COMPANY
ELECTRONICS LABORATORY
SYRACUSE, NEW YORK

Best Available Copy

TABLE OF CONTENTS

Section		Page
I.	PURPOSE	1
II.	ABSTRACT	2
III.	CONFERENCES AND REPORTS	3
	A. Conferences	3
	B. Reports	4
IV.	FACTUAL DATA	5
	A. Power Dissipation Study	5
	1. Deleterious Effects of Power Dissipation	5
	2. A General Approach to the Problem	6
	3. The Factors which Directly Affect Power Dissipation	12
	4. A Practical Approach to the Design of the DCTL-NOR	19
	5. DTL-NOR Circuit Design	52
	B. Optimum Tolerance Selection	82
	C. Terminal Parameter Measurements	114
	D. Adjustability	131
V.	IDENTIFICATION OF KEY PERSONNEL	146
	APPENDIX B-1 Long Term Versus Short Term Reliability of Circuits and Systems	155

TABLE OF CONTENTS - continued

Section		Page
APPENDIX B-2	Circuit Design	169
APPENDIX B-3	Circuit Analysis	194
APPENDIX B-4	Parameter Confidence Design Method	207
APPENDIX C-1	Terminal Parameter Measurements	221

LIST OF ILLUSTRATIONS

Figure No.		Page
1.	Hypothetical Results of Optimum Circuit Designs of a Specific Circuit Topology.....	9
2.	a. Idealized Binary Signal Source-First Category	15
	b. Idealized Binary Signal Source-Second Category	15
3.	Variation of Power With Non-Optimal Design...	18
4.	DCTL-NOR Circuit Configuration.....	20
5.	The Result of Paralleled Operation of Two Diode Type Loads with Different Voltage Shifts	22
6.	DCTL Signal Source Driving Two Diode-Type Loads...	24
7.	a. DCTL "Source-off" Condition (Static).....	27
	b. DCTL "Source-on" Condition (Static).....	27
8.	Graphical Determination of I_{bn} for the DCTL-NOR...	31
9.	2N708 Current Gain Characteristics.....	33
10.	2N708 Base-Emitter Characteristic.....	34
11.	2N708 Incremental Waste Current.....	35
12.	Superposition of β Characteristic and Design Equation at Minumum Temperature of 25°C	37
13.	Available Ψ VS. I_{bn} At Minimum Temperature of 25°C..	38
14.	Superposition of β and Design Equations at 25°C and Fanout of 3.....	40
15.	Maximum Available Ψ VS. I_{bn} at 25°C.....	41
16.	Maximum Available Ψ VS. Minimized Power at 25°C	42
17.	Superposition of 2N708 β Characteristic and Design Equation.....	44

LIST OF ILLUSTRATIONS - continued

Figure No.		Page
18.	Superposition of β Characteristic and Design Equations	45
19.	Available ψ VS. Base Current At $-55^{\circ}C$	46
20.	Minimized Power Dissipation At $-55^{\circ}C$	47
21.	Frequency of Operation VS. Power Dissipation	49
22.	Maximum Frequency of Operation VS. Power Dissipation	50
23.	Frequency VS. Power At Different Confidence Levels	51
24.	"NAND" Gate	53
25.	Variation of Power For Non-Optimum Choice	57
26.	Design Problem From Geometric Point-of-View	61
27.	Approximate Equivalent Circuits for Static Design	64
28.	Design Region for Conducting State	68
29.	Design Region for Non-Conducting State	72
30.	Compatible Design Region for Two States of Circuit	75
31.	Probability of Drift Failure Curve (Specification $y_1 \geq A$)	83
32.	Relay Circuit	84
33.	Probability Density Functions of R and E	86
34.	Saturating Base Returned Flip-flop Configuration	89
35.	Power Dissipation VS. Percent Tolerance	92
36.	Probability of Non-Drift VS. Temperature Range	93
37.	Component Distributions of Four Vendors	96
38.	T_{op} VS. T_o to T_X	101
39.	Probability of Success VS. Percent Tolerance	103

LIST OF ILLUSTRATIONS - continued

Figure No.		Page
46.	Probability of Success VS. Percent Tolerance.....	104
47.	Probability of Success VS. Percent Tolerance.....	105
48.	Probability of Success VS. Time.....	106
49.	Probability of Success VS. Time.....	107
50.	Probability of Success VS. Time.....	108
51.	Probability of Success VS. Time.....	110
52.	Probability of Success VS. Time.....	111
53.	Probability of Success VS. Time.....	112
54.	Flip-flop With 7 Available Terminals.....	118
55.	Equivalent Circuit.....	119
56.	Circuit for Determining β_o of T_1.....	122
57.	Flip-flop with 6 Available Terminals.....	123
58.	Circuit for Determination of β_o of T_1.....	124
59.	Flip-flop With 8 Available Terminals.....	126
60.	Determination of C_3.....	127
61.	Low-pass Voltage Transfer Function.....	132
62.	Band-pass Voltage Transfer Function.....	132
63.	Basic Digital Filter.....	134
64.	Low Frequency Switching Waveform Generation.....	135
65.	Basic Waveform Generating Circuits.....	137
66.	Shift Register Connection Diagram.....	138
67.	Digital Filter Circuit.....	139
68.	Noise Balancing Network.....	141

LIST OF ILLUSTRATIONS - continued

Figure No.		Page
63.	Fundamental Component of Commutating Noise as a Function of Center Frequency.....	142
64.	Digital Filter Voltage Transfer Ratio at 200 kc Center Frequency with 160 Cycle Theoretical Bandwidth.....	143
65.	Digital Filter Voltage Transfer Ratio at 1 Mc Center Frequency with a 2 kc Theoretical Bandwidth	144
66.	Voltage Transfer Ratio at Center Frequency as a Function of Center Frequency.....	145

LIST OF TABLES

Table No.		Page
1.	Synthesis Procedure - Nand Gate.....	76
2.	Design Example.....	78
3,	Date (Constants and Specifications) for the Computer Program.....	90
4.	Normal Circuit Resistance Values.....	91
5.	Temperature Range where Circuit Will Hold Up.....	95
6.	Computed T_{op}, Interpolated P(D), and λ.....	93

I. PURPOSE

The purpose of this contract, as outlined in technical requirements for PR and C No. 61-ELP/R-4103, is to carry out studies leading to specific information and criteria which can be used in evaluating the potential merits and limitations of various approaches to microelectronics. Phase I of the program is divided in the following portions:

Power Dissipation Study - The purpose is to develop realistic sets of specifications for commonly required circuit functions. A determination will be made of the minimum power levels at which such circuits can be operated satisfactorily and the "trade offs" which are involved in lowering the power level.

Reliability - One purpose is to determine the relationship between drift and catastrophic failures and their effects on system reliability. The optimum tolerance point for a system will be determined as well as the practical limits of complexity of integrated structures for a given design reliability.

The effect of individual component or device variations on the terminal performance of a circuit will be studied with a view to developing a procedure for evaluating the internal component state of an integrated circuit.

Adjustability - The purpose is to study means of decreasing the number of external adjustments for microelectronic circuits sensitive to component variations. The use of techniques to electronically adjust circuit characteristics will also be analyzed.

II. ABSTRACT

A number of investigations have been carried out to assess the merits and limitations of the various forms of microelectronic circuitry. Specific tasks have been conducted to provide design criteria and information with the objective of improving microelectronic design and evaluation procedures. Solutions are given to the problem of how to design minimum power dissipation circuits. The effects of power dissipation, circuit tolerance, component tolerance and temperature on circuit reliability are considered. Solutions to the problem of attaining maximum circuit reliability are presented. It is shown how to evaluate various forms of microelectronic circuitry when only a limited number of terminals are available. The results of studies in the area of adjustability are presented.

III. CONFERENCES AND REPORTS

A. CONFERENCES

Date: 21 July 1961

Place: General Electric Electronics Laboratory, Syracuse, New York

In Attendance: J. Meindl, USASRDL
J. Hohmann, USASRDL
J.J. Suran, E. Lab., General Electric Co.
J.A.A. Raper, E. Lab., General Electric Co.
R.T. Loew, HMED, General Electric Co.

Subject: Discussion of specific work to be undertaken during the first year of the Solid State Microelectronics Program.

Date: 4 December 1961

Place: General Electric Electronics Laboratory, Syracuse, New York

In Attendance: J. Hohmann, USASRDL
J.J. Suran, E. Lab., General Electric Company
J.A.A. Raper, E. Lab., General Electric Company
L.J. Ragonese, E. Lab., General Electric Company
G.H. Danielson, E. Lab., General Electric Company
R.E. Warr, E. Lab., General Electric Company

Subject: Discussion of progress, problem areas and program plans

Date: 23 February 1962

Place: USASRDL, Fort Monmouth, New Jersey

In Attendance: J. Hohmann, USASRDL
A. Bramble, USASRDL
R. Farley, USASRDL
J.J. Suran, E. Lab., General Electric Company
J.A.A. Raper, E. Lab., General Electric Company
L.J. Ragonese, E. Lab., General Electric Company
R.E. Warr, E. Lab., General Electric Company

Subject: Discussion of Progress

1. Minimum power dissipation study of NAND and D.T. circuits.
2. Optimum design tolerance study.
3. Terminal parameter measurements.
4. Digital filter study.
5. Amplifier redundancy

Date: 5 June 1962

Place: General Electric Electronics Laboratory, Syracuse, New York

In Attendance: A. Bramble, USASRDL
R. Farley, USASRDL
J.J. Suran, E. Lab., General Electric Company
J.A.A. Raper, E. Lab., General Electric Company
L.J. Ragonese, E. Lab., General Electric Company
P.W. Becker, E. Lab., General Electric Company
G.H. Danielson, E. Lab., General Electric Company
R. Loew, HMED, General Electric Company

Subject: Discussion of Progress

B. REPORTS

Monthly Letter Report No. 1 (1 July through 1 August 1961)
Monthly Letter Report No. 2 (1 August through 1 September 1961)
Monthly Letter Report No. 2 (1 September through 1 October 1961)
Quarterly Report No. 1 (1 July through 1 October 1961)
Monthly Letter Report No. 4 (1 October through 1 November 1961)
Monthly Letter Report No. 5 (1 November through 1 December 1961)
Monthly Letter Report No. 6 (1 January through 1 February 1962)
Quarterly Report No. 2 (1 October through 1 January 1962)
Monthly Letter Report No. 7 (1 February through 1 March 1962)
Monthly Letter Report No. 8 (1 April through 1 May 1962)
Quarterly Report No. 3 (1 February through 1 May 1962)
Monthly Letter Report No. 9 (1 May through 1 June 1962)
Monthly Letter Report No. 10 (1 June through 1 July 1962)

IV. FACTUAL DATA

A. POWER DISSIPATION STUDY

1. Deleterious Effects of Power Dissipation

Some of the deleterious effects of increased power dissipation in microelectronic systems are outlined here for the purpose of background material.

As a typical system, let us consider a microelectronic digital computer composed of a large fixed number of similar digital logic gain circuits. These circuits are interconnected in some arbitrary logical array. Let us further assume that the computer is to completely fill an appropriate spherical or cubical container.

Thermodynamically, the operating computer is a heat generator whose output is equal to the sum of the heat generated by all the similar circuits. If the external surface of the computer is to be maintained at some nominal temperature, then heat must be removed from the surface at the same rate at which it is being generated. Thus, the size and complexity of the cooling system for the given computer is directly related to the dissipation of the individual logic gain circuit.

But the rate at which the cooling system must transfer heat from the surface of the computer is exactly equal to the power which must be furnished by the power supplies of the computer. Thus, higher circuit power dissipation results in the need for more elaborate power supplies.

For the particular dimensions and heat conductivity involved, there will be a temperature differential between a circuit on the surface of the computer and one which is closest to the center of the computer. This temperature differential is directly related to the power dissipation of a basic circuit. Depending on the specific size, thermal conductivity, and circuit power dissipation of our computer, the temperature differential could be as low as less than one to greater than 100 centigrade degrees.

Electronic components including resistors, diodes and transistors show appreciable variation in terminal parameters as a result of temperature variation on the order of tens of degrees. Thus, a high temperature differential within the computer introduces a greater randomness into the parameter values. Since all the circuits in the computer are designed around the same nominal values, temperature differential increases the probability of drift failure within the computer.

There is strong evidence that the catastrophic failure rate of components is directly related to their respective absolute temperature of operation. Greater circuit power dissipation results in a greater temperature differential within the given computer. For a certain maintainable computer surface temperature, a greater temperature differential implies a higher ambient temperature for the more centrally located circuits. Thus, higher circuit power dissipation results in a higher catastrophic failure rate for the internal circuits of the computer.

In summary, increased power dissipation can offset many of the space and weight advantages of microelectronics by requiring large cooling systems and power supplies. Furthermore, the probability of drift and catastrophic failure are enhanced by increased power dissipation.

2. A General Approach to the Problem

If it is agreed that power dissipation is to be minimized, the question then arises as to what extent power dissipation in a circuit can be decreased, if at all, without affecting its usefulness. In order to evaluate the change in usefulness of a circuit as a result of changing the power dissipation, usefulness must be specified in terms of measureable quantities. We choose to describe the usefulness of a digital circuit in terms of herein defined "operational properties."

a. The Operational Properties

The operational properties of a digital circuit may be defined as those which are of direct interest to the system designer. The five operational properties are: Logic capability; maximum fan-out;

maximum frequency of operation; maximum number of circuits per unit volume; and reliability. These operational properties are not necessarily independent of one another.

Logic capability, as defined here, is purely a function of the circuit topology. Factors which affect logic capability include: number of logic levels; fan-in; inversion; and availability of both normal and complemented outputs.

Maximum fan-out is the number of loads to which a logic gain circuit can supply a logical decision. The loads are inputs of similar logic gain circuits.

Maximum frequency of operation is determined by the rise, fall, delay and recovery times of the output signal as a result of an input signal or signals from similar logic gain circuits.

The maximum number of circuits per unit volume is a function of the thermal interconnection scheme, the power dissipation of a circuit, the maximum temperature allowable in the computer, and the computer heat sink temperature.

Reliability is herein used in the conventional sense. This project will concentrate on the aspects of reliability which can be affected by the circuit parameter design.

b. The Idealized Design Problem

The topological design of a digital circuit is largely in nature. It depends primarily on the ingenuity of the designer and the type of application for which it is needed. This project, therefore, will deal primarily with the problems in the parameter design of specific circuit topologies. If the circuit topology is presupposed, then logic capability, as we have defined it, is fixed and is not a design variable. The remaining four operational properties are, therefore, of major interest to the designer.

In the selection of parameter values for a given circuit topology, the designer might consider the parameters as variables and the operational properties as constraints which the circuit must fulfill.

In order to utilize this approach, separate equations would be necessary for : maximum fan-out; maximum frequency of operation; circuit power dissipation; and circuit reliability in terms of the circuit parameters. The equations for : maximum fan-out; maximum frequency of operation; and circuit reliability would each be set equal to an arbitrary constant. A calculus minimization problem could then be solved for minimum power dissipation within the operational property constraints. If a realizeable solution existed, then the optimum parameter values thus would be found for the given set of arbitrary constants. Knowing the parameter values, the actual minimum power dissipation could be easily computed.

The assumed value of reliability and fan-out could be held constant while the assumed maximum frequency of operation could be arbitrarily set at several other values. For each change, a new set of parameter designs would be found.

The whole procedure could then be repeated for other values of fan-out. Figure 1 shows the hypothetical results of the above computations. In general, each point on the curves refers to a different set of parameter values. The set of curves would explicitly indicate to the system designer what the trade-off is between packing density (power dissipation) and maximum frequency of operation for a fixed circuit reliability as applied to a specific circuit topology. Once the system designer has decided on a particular compromise by choosing a point on one of the curves, he could refer to the library of designs which generated the curves for the particular circuit to fulfill his particular demands.

It is certainly true that an infinite number of designs would be necessary to provide all the possible choices of the system designer. On the other hand, assuming relatively smooth curves, about five design points should be sufficient to describe each curve. Once the curves are described, the system designer is able to predict the realizeable trade-offs even before the specific circuit is actually designed. The design of a previously unrecorded point on an established curve should not be very difficult.

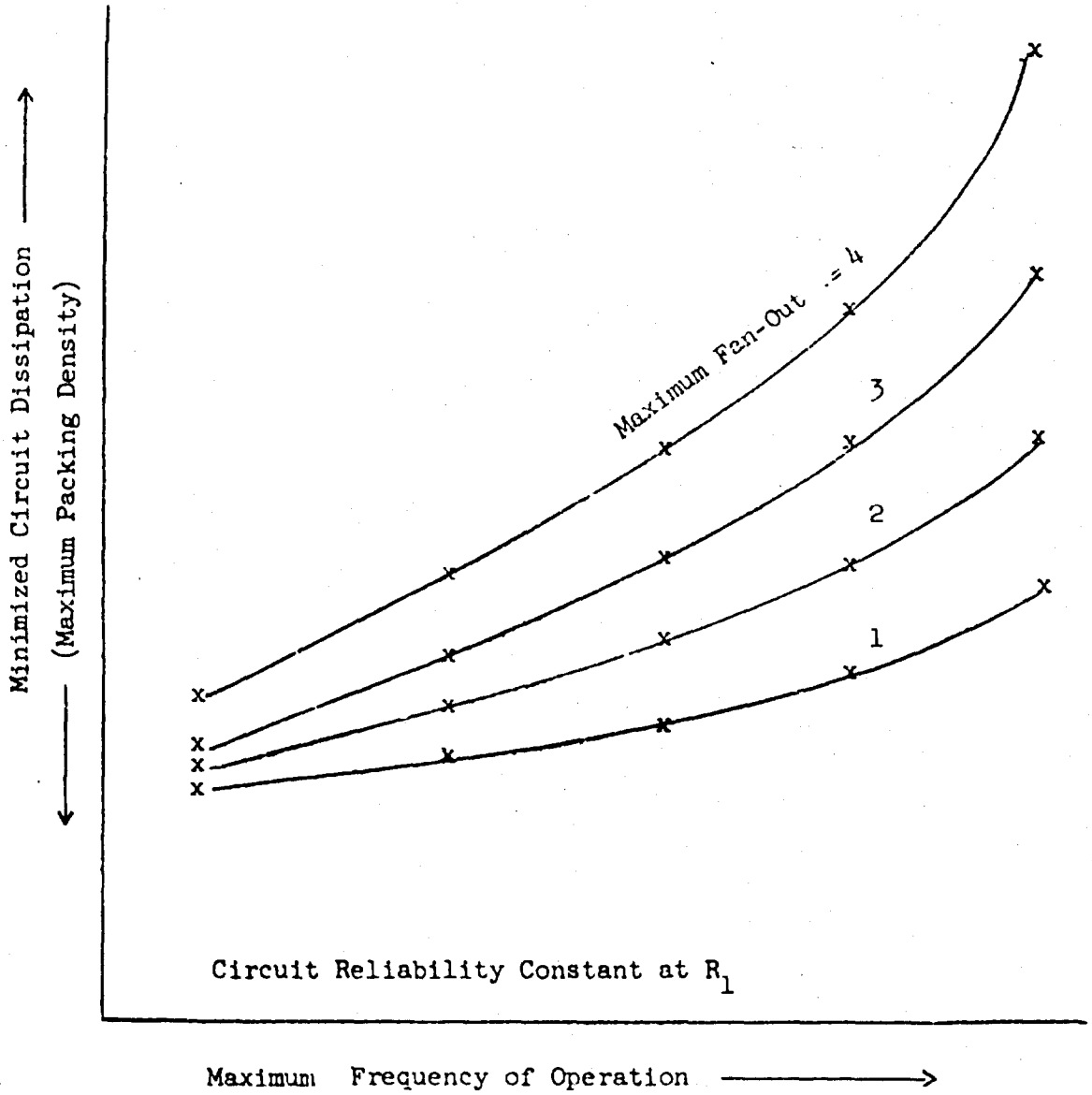


Figure 1. Hypothetical Results of Optimum Circuit Designs of a Specific Circuit Topology.

It will be noted that the title to this section contains the word "idealized." The objective of this section was to illustrate the following ideas:

1) In spite of all the factors which we will later consider for practical circuit design, they are only important in that they effect the relatively few operational properties.

2) If we could obtain equations for the operational properties in terms of the parameters; if the calculus or algebra doesn't get too difficult to solve; and if we choose reasonable arbitrary values of three of the operational properties; then the design problem is a straightforward process. The problem is that each of these "ifs" are easier said than done.

3) Even if the above "idealized" approach is impossible, calculus minimization techniques should be used wherever possible in our design. As will be shown later, the results of this technique can be very useful and general in nature.

4) Power dissipation can only be decreased to the extent that the circuit is still useful or functioning properly. Minimum power dissipation is meaningful only relative to specific operational properties.

5) It appears that information of the type hypothesized in Figure 1 will eventually have to be generated if power dissipation studies are to be useful.

6) If the operational properties are to be realized, there must be at least as many parameter variables as there are operational constraints.

c. The Fundamental Properties

It is customary to consider basic logic gain digital circuits in terms of a set of fundamental properties. These properties include: logic capability; maximum fan-out; maximum frequency of operation; power dissipation; isolation; directionality; interconnection interaction; randomness; limiting; threshold level; signal amplitude; and stability. The first three are identical with the similarly named operational properties. Power dissipation is extremely closely related to maximum number of circuits per

unit volume. The last eight are all related to the operational property named reliability. Although these eight properties are not the only factors which affect reliability, they are the only variables through which the circuit designer may influence reliability.

Isolation pertains to the degree of signal propagation between different input channels of the same logic gain circuit.

Directionality pertains to the degree of undesired signal propagation from the output to the input of a logic gain circuit.

Interconnection interaction pertains to the degree of undesired signal propagation from one communication line to another line.

Randomness is a property which permeates any practical circuit. The values of resistance, the current amplification factor of the transistor, the threshold level, the signal amplitude, and many other circuit parameters all have actual values which are a varying percentage away from some nominal value. Some device parameters are much more random than others. Were it not for randomness, the signal amplitude could be appreciably decreased.

Limiting is the restandardization of the signal extremities corresponding to a logical one or a zero.

Threshold level is the property of a digital circuit which allows it to properly amplify information signals while attenuating or rejecting certain noise signals.

Signal amplitude commonly refers to the minimum difference of extremities in the signal which is used to communicate from one circuit to another. One can also speak of threshold signal amplitude as the minimum difference of extremities in the signal which appears at the threshold point.

Stability means many things to many people. We will define it as the absence of any condition whereby a logic gain circuit supplies erroneous information to its loads at least partially as a result of regeneration within the circuit. Two examples of instability are thermal runaway and electrical oscillation due to unintentional positive feedback.

The question may arise as to the reason for defining two sets of circuit properties - the operational and the fundamental. The reason is that there are relatively few operational properties while more than twice as many fundamental properties. The fundamental properties are only important in that they affect the operational properties. If we were to apply arbitrary values for each of the fundamental properties, then each fundamental property would constitute a constraint. Therefore, we would need at least as many variable parameters as there are fundamental properties. Most logic gain circuits do not have enough variable parameters to correspond to the number of fundamental properties. Therefore, a solution would be impossible.

As was indicated previously, the fundamental properties of: isolation, directionality, interconnection interaction, randomness, limiting, threshold level, signal amplitude, and stability are all related to drift reliability as defined under operational properties. One of the objectives of this program has been to quantitatively describe this relationship.

It may qualitatively be seen that isolation, directionality, and interconnection interaction are similar types of signals. Their cumulative effect is a voltage or current noise signal as seen at the threshold point in the circuit. Randomness in limiting levels along with randomness in the components which "transmit" the limited signal to the threshold point introduce ambiguity as to whether the transmitted signal is "above" or "below" the threshold level. Randomness in the threshold level introduces a further ambiguity. It is possible to adjust the signal amplitude sufficiently to overcome the "noise" effects of isolation, directionality, interconnection interaction, and randomness.

3. The Factors which Directly Affect Power Dissipation

The factors which directly affect power dissipation are: basic circuit topology; signal amplitude; maximum frequency of operation; and the extent of power minimization.

a. Basic Circuit Topology

The basic circuit topology is assumed predetermined. However, it should not be forgotten that an optimized version of one circuit may in general dissipate more or less power than an optimized version of another circuit topology even though both have the same remaining operational properties.

b. Signal Amplitude

The signal amplitude is determined by reliability considerations. The greater the signal amplitude, the greater must be the current that charges capacitive portions of the circuit at a given maximum frequency of operation. Since the power supply voltages are directly related to the signal amplitude, the greater signal amplitude results in larger supply voltages. Since the ultimate source of the currents are the power supplies, and since power is directly related to the supply voltages and currents through them, then it appears, at least empirically, that larger signal amplitudes must result in higher power dissipation. This question will be further investigated.

c. Maximum Frequency of Operation

Using the same arguments as the last paragraph, for a fixed signal amplitude, the power dissipation must increase with increasing speed of operation. In this case the same capacitive charge must be supplied in less time - thus currents must be higher.

d. Power Minimization - The Bi-State Design

As we have mentioned, the function of a logic gain circuit is to arrive at a logical decision and then to deliver the decision or its complement to a certain number of loads. In delivering the decision to the loads, the circuit is acting as a signal source. There are at least two categories of signal sources in digital circuits.

Best Available Copy

The first category is schematically shown in Figure 2a. The two switches are never simultaneously closed. If the top switch closed and the bottom switch open corresponds to a logical one, then reversing the condition of both corresponds to a logical zero. This category is recognized by the fact that, neglecting battery and switch resistance, the logic gain source has no internal dissipation in either state. Since most electronic switching devices fall in the category of single pole single throw switches, this category of logic gain circuit usually requires at least two active devices.

Probably the vast majority of logic gain digital circuits today fall in the second major category illustrated in Figure 2b. As shown in the Figure, in state no. 1, the battery supplies current I_{L_1} to the load. At the same time, there is a voltage divider action between the load resistance and R_s such as to supply V_L to the loads. In state no. 2, the switch closes and the loads are essentially isolated from the battery. It will be seen that in both states, current flows through R_s and therefore there is power dissipated in the signal source.

Usually V_L and I_{L_1} are predetermined by the requirements of the loads. For given values of V_L and I_{L_1}, if R_s is decreased in order to decrease the source power dissipation in state no. 1, then the source dissipation in state no. 2 will increase. What, then, are the optimum values of R_s and E_s such that I_{L_1} and V_L are supplied to the load in state no. 1 and minimum power is dissipated by the signal source in state no. 2? A calculus minimization attack to the problem readily yields the answers as shown below:

In state no. 1:

$$I_{L_1} = \frac{E_s - V_L}{R_s}$$

In state no. 2:

$$I_2 = \frac{E_s}{R_s} = \frac{E_s I_{L_1}}{E_s - V_L} \quad \text{since } R_s = \frac{E_s - V_L}{I_{L_1}}$$

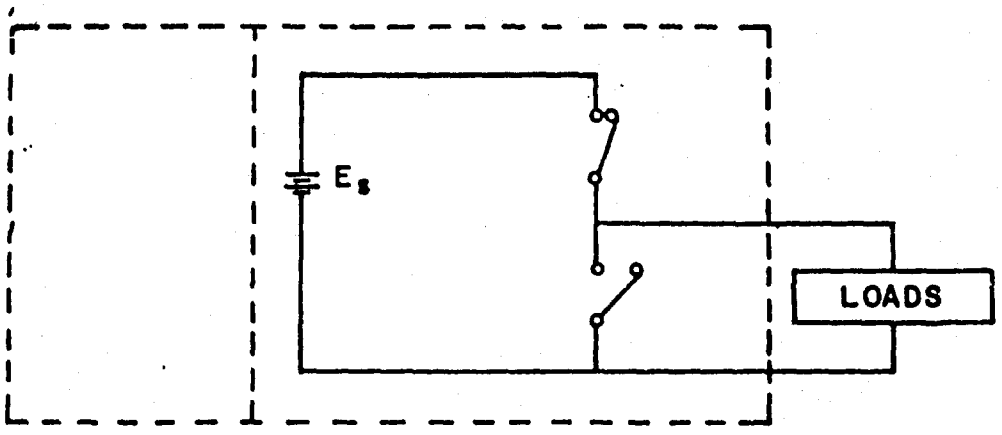


Figure 2a. Idealized Binary Signal Source - First Category

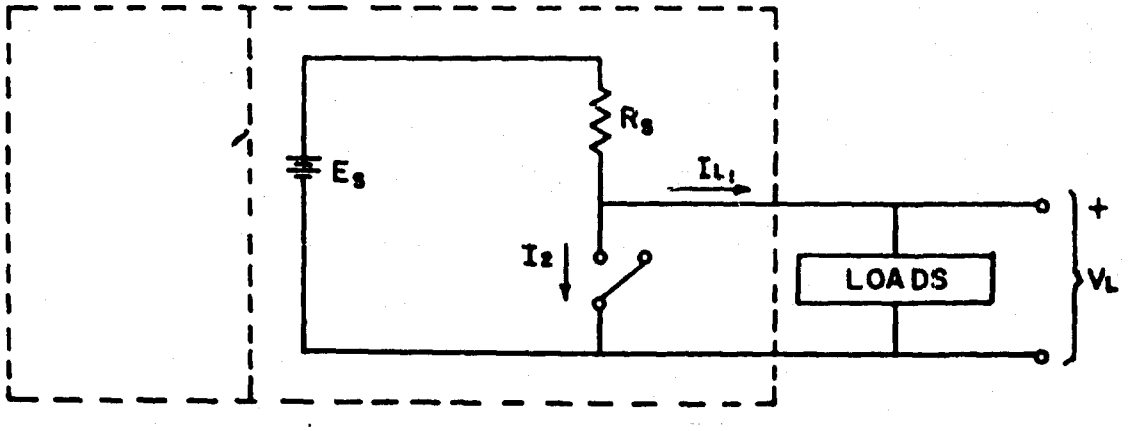


Figure 2b. Idealized Binary Signal Source - Second Category
(Shown in State No. 1)

$$\text{Power in state no. 2} = P_2 = E_s I_2 = \frac{E_s^2 I_{L_1}}{E_s - V_L}$$

Since we wish to find a minimum, we set the derivative of power with respect to E_s equal to zero:

$$\frac{dP_2}{dE_s} = \frac{E_s I_{L_1} (E_s - 2V_L)}{(E_s - V_L)^2} = 0$$

$$\therefore \quad E_s - 2V_L = 0$$

$$E_s = 2V_L$$

but

$$R_s = \frac{E_s - V_L}{I_{L_1}} = \frac{V_L}{I_{L_1}}$$

Thus E_s and R_s are seen to be simply related to the load requirements.

The above solution yields an optimum value of E_s for the given load conditions. It will now be shown how power dissipation increases for non-optimal values of E_s.

$$P_2 = \frac{E_s^2 I_{L_1}}{E_s - V_L}$$

Minimum Power in State no. 2

$$= \underline{P_2} = \frac{(2V_L)^2 I_{L_1}}{2V_L - V_L} = 4 V_L I_{L_1}$$

$$\frac{P_2}{\underline{P_2}} = \left(\frac{E_s^2 I_{L_1}}{E_s - V_L}\right)\left(\frac{1}{4 V_L I_{L_1}}\right) = \frac{E_s^2}{4 V_L (E_s - V_L)}$$

let us define $E_s = k V_L$

$$\therefore \quad P_2 = \left(\frac{k^2}{4 (k - 1)}\right) \underline{P_2}$$

let us now define $K = \frac{k^2}{4(k-1)}$

$$\therefore P_2 = K \underline{P_2}$$

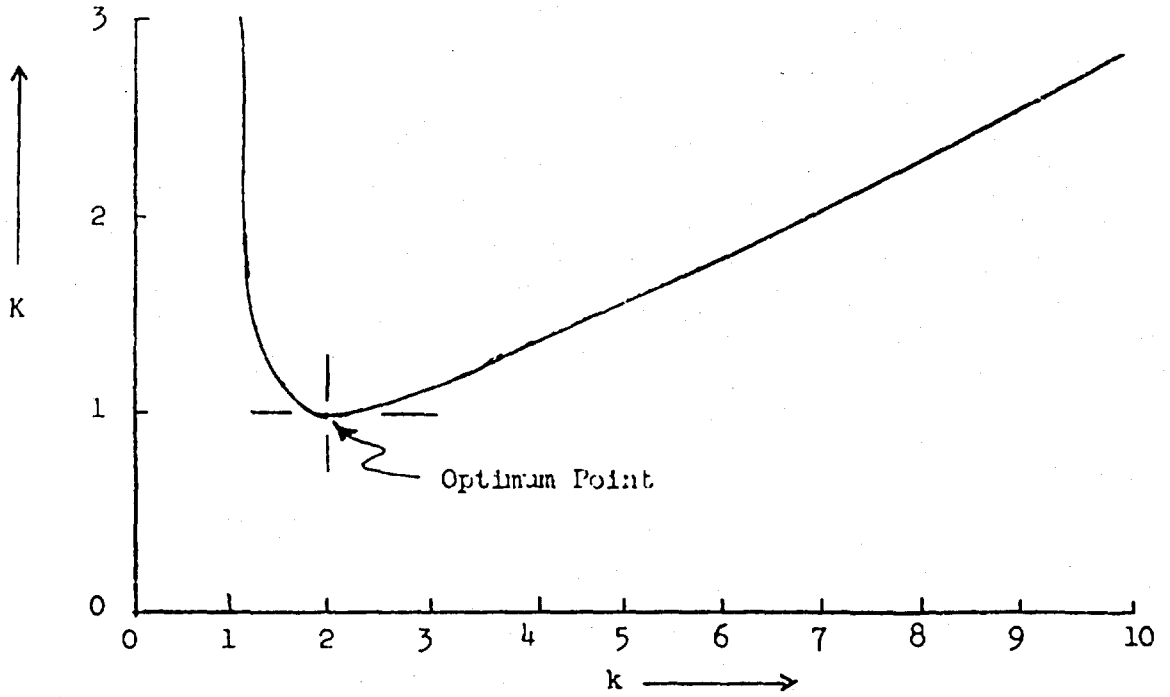
A plot of K versus k is shown in Figure 3. This curve shows that the signal source can easily dissipate two or three times the minimum required power for the given load conditions if not optimized.

In the above solution, the power in state No. 2 was minimized. If the circuit is switching back and forth between states No. 1 and No. 2, the circuit could be designed to minimize the sum of the power dissipation in both states. The solution to this problem yields:

$$E_s = 1.707\ V_L$$

$$R_s = \frac{.707\ V_L}{I_{L_1}}$$

This bi-state design technique is one relatively general example of design procedures which can result in the minimization of power dissipation while achieving certain operational property requirements. This bi-state design is generally applicable to designing "second category" signal sources. Where the designer has the flexibility to influence the load, somewhat similar procedures can also be applied as will be shown later in conjunction with the DTL-NOR circuit.



$$P_2 = K \underline{P_2}$$

$$K = \frac{k^2}{4\,(k-1)}$$

$$E_s = k\, V_L$$

Figure 3. Variation of Power With Non-Optimal Design.

4. A Practical Approach to the Design of theDCTL-NOR

The DCTL-NOR circuit shown in Figure 4 is the subject of present consideration. The power dissipation in each of these circuit types can only be decreased within the framework whereby they fulfill a particular set of operational properties. The desired operational properties include maximum fan-out (fan-in), maximum frequency of operation, and a particular probability of error-free operation.

From the point of view of the circuit designer, the power dissipation of a circuit reflects the cumulative effects of the circuit component characteristics, the desired operational propertics of the circuit, and the degree of power minimization.

a. Discussion of the Problem

The DCTL-NOR circuit shown in Figure 4 has received wide attention in the microelectronic field due to its physical simplicity. In this circuit the threshold function is achieved through use of the transistor base to emitter V-I characteristic. The base to emitter V-I characteristic is of the "diode-type". In the process of achieving logic fan-out, it is necessary to connect several of the threshold devices in parallel with one another. These, as a group, constitute the load as seen by the previous information signal source. Ideally, the signal source would supply the same amount of current to each of the threshold points. It will be seen, however, that even relatively small variations in the threshold characteristics can result in radically different current being supplied to the different threshold points.

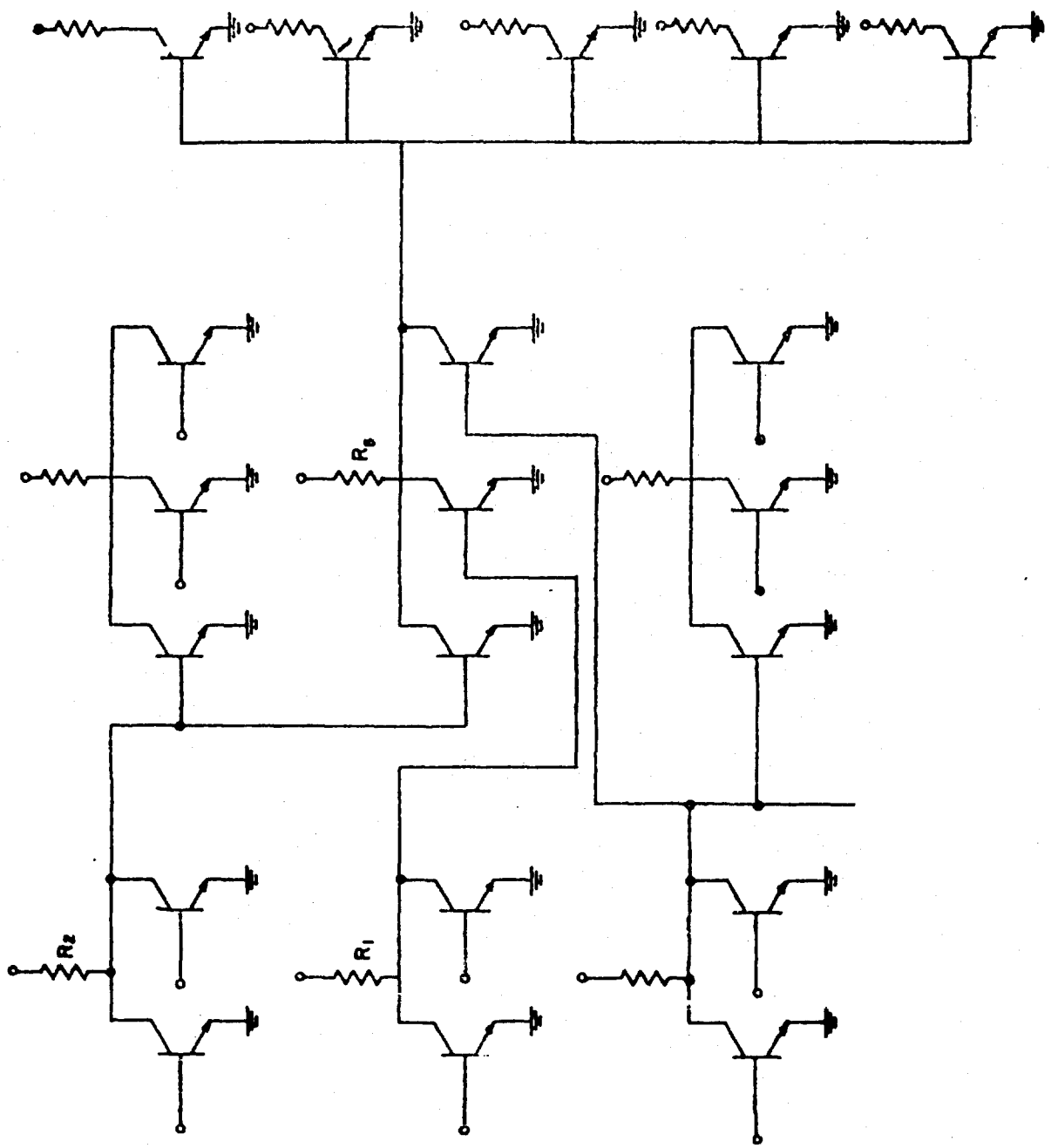


Figure 4. DCTL-NOR Circuit Configuration

The Effect of Connecting Diode-Type Devices in Parallel

Consider the characteristics of Figure 5. Line $\overline{ABM}$ represents the V-I characteristic of an idealized diode-type load. Line $\overline{ACN}$ represents the V-I characteristics of another idealized diode-type load, which has the same "forward" and "backward" resistance values as the first one, but which has a different voltage "break point". If the devices which correspond to the two characteristics are connected in parallel, their combined characteristic is represented by line $\overline{ABGL}$. If we require that at least three units of current be supplied to each of the diode-type loads by some source, it is seen that the source must supply at least a voltage corresponding to $\overline{AP}$ to the combined loads. If this is to be true, the V-I characteristic of the source must intersect the combined load characteristic somewhere along $\overline{JL}$. For minimum power dissipation in the combined load within the constraint that each load be supplied at least three units of current, the point J on line $\overline{JL}$ would of course be selected as the intersection point. If this is carried out, it is seen that a current $\overline{FP}$ would be supplied to one load while a current corresponding to $\overline{OP}$ would be supplied to the other load. For the example shown, one load would be supplied three times the minimum current.

It is interesting to note that if the minimum current requirement is decreased to some finite value approaching zero, the power supplied to one load approaches zero while that of the other load approaches the product of $\overline{AC}$ and $\overline{GC}$. The distance $\overline{GC}$ corresponds to a "waste" current. The waste current is a function of the forward conductance Y_f and the voltage difference ΔE_{bp} between the maximum voltage device and the other device under consideration:

$$\text{Waste Current} = (Y_f)(\Delta E_{bp})$$

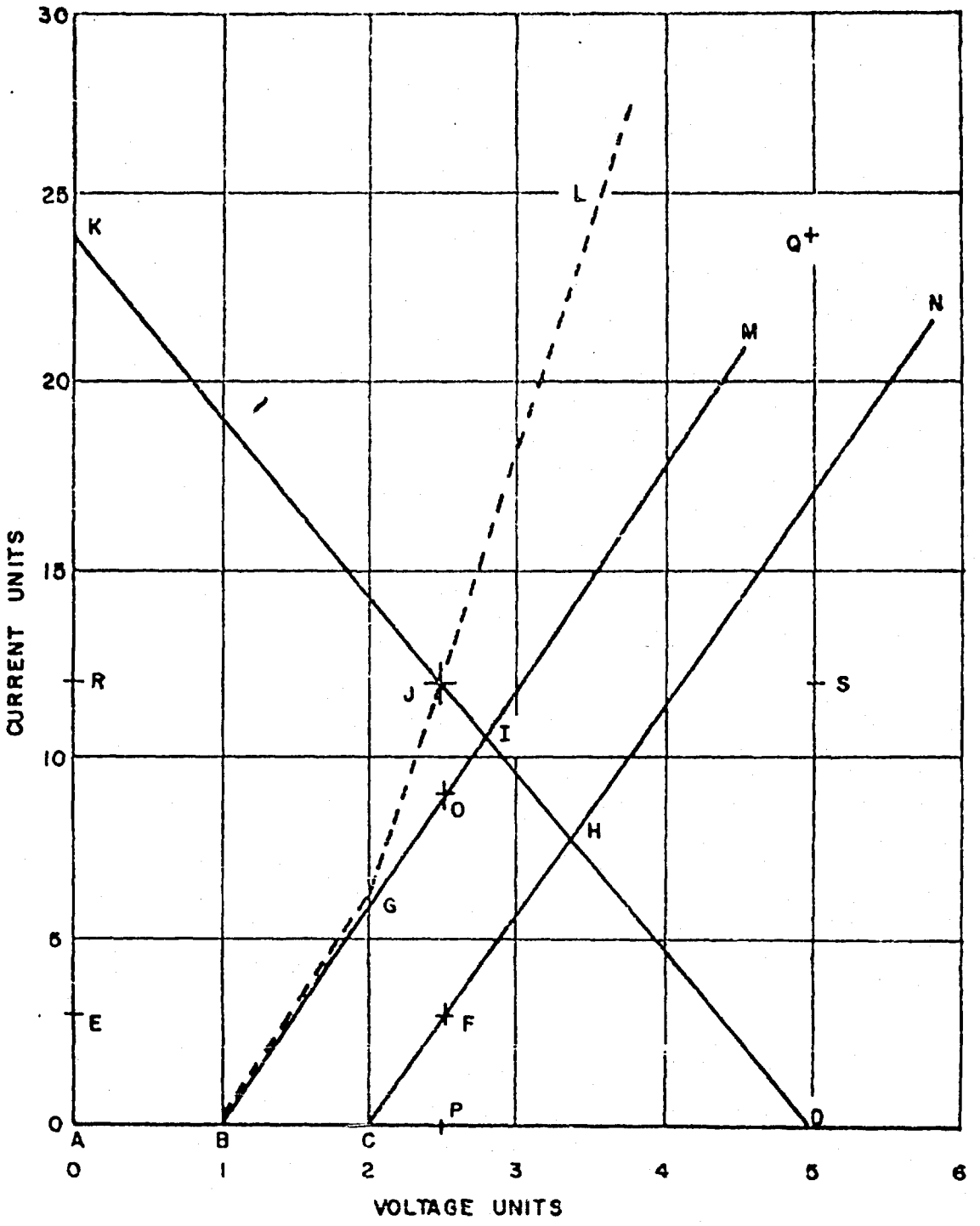


Figure 5. The Result of Paralleled Operation of Two Diode Type Loads with Different Voltage Shifts

If n_o loads selected randomly as having either $\overline{ABM}$ or $\overline{ACN}$ characteristics are connected in parallel, the worst case necessary waste current is given by:

$$I_w = \text{Total waste current} = (n_o - 1)(Y_f)(\Delta E_{bp}) .$$

Thus, even though the minimum required individual load current may be made to approach an extremely small positive value, the source which supplies the m-paralleled load must be capable of supplying the waste current I_w at a voltage greater than $E_{bp\ max}$ - the maximum breakpoint voltage. The product of the maximum breakpoint voltage and the waste current represents an absolutely minimum value of power which must be supplied by the driving signal source. This power is essentially wasted. In practical situations, this "waste" power may represent a major portion of the total load power dissipation.

The DCTL Signal Source Driving Diode-Type Loads

The previous section considers the effect of the parallel connection of two diode-type loads. Let us now consider that the characteristics of Figure 5 represent the base to emitter characteristics of the two load transistors of Figure 6. The two loads are being driven by a DCTL signal source.

Let us consider the following design problem:

Given:

(1) Two parallel connected loads with characteristics as shown in Figure 5.

(2) A signal source as shown in Figure 6.

(3) Each load must be supplied a minimum of 3 current units.

(4) The signal source presents essentially a short circuited output in the "source on" condition.

Find:

The values of E_s and R_s which will minimize the power dissipated in the signal source in its "on" state.

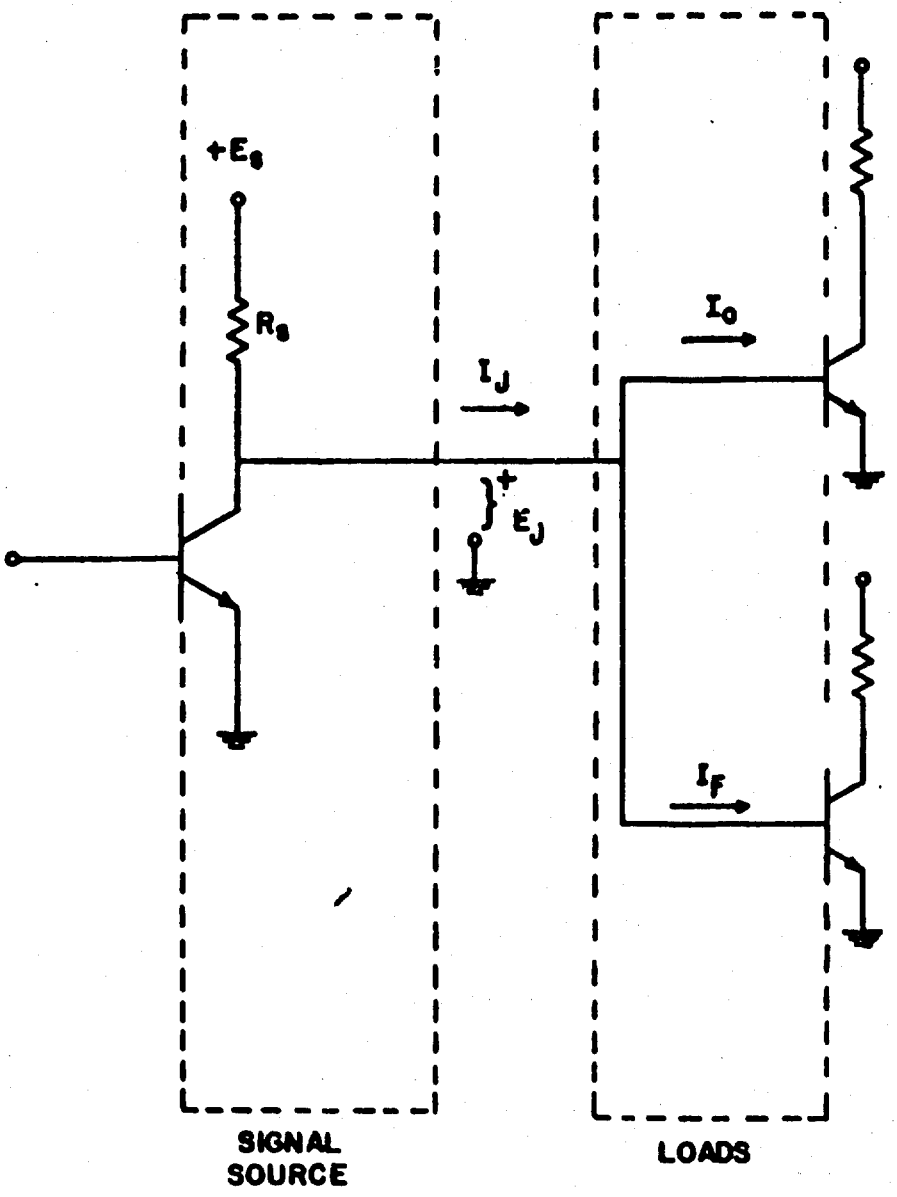


Figure 6. DCTL Signal Source Driving Two Diode-Type Loads

Solution: (using Figure 5)

(1) The minimum load current requirement establishes E_p as the minimum acceptable steady state output when the source is in the "off" condition.

(2) The paralleled diode characteristics establish $I_J = I_o + I_F$ as the minimum acceptable current to be supplied by the signal source in its "off" condition.

(3) It is seen that the signal source load line must intersect the load characteristics somewhere along line $\overline{JL}$. Minimized power considerations establish point J as the proper choice of intersection point.

(4) Once point J is selected the Bi-State Nominal Design derived [illegible] establishes $E_s = 2\ E_J$ which determines the point D in Figure 5.

(5) The resistor $R_s = E_J/I_J$ establishes the source load-line $\overline{KJD}$.

Some Graphical Observations:

(1) The rectangular area $\overline{AKQD}$ represents the "signal source on" source power dissipation "power rectangle".

(2) Any other choice of E_s and R_s which establish a load line through point J would have had a higher "signal source on" power dissipation. The new "power rectangle" would have a greater area.

(3) The rectangle $\overline{ARJP}$ represents the power delivered to the load in the "source off" condition.

(4) The minimized "source on" dissipation is FOUR times the maximum power which the "source off" will be required to supply the combined load! This is an extremely important fact! Another way of saying it is that the optimum "source on" power dissipation is four times the "source off" power capability - not necessarily the power that is actually being dissipated in a particular instance.

(5) Point D must be designed to correspond to the minimum expected value of E_s and the slope of $\overline{KJD}$ must be designed to correspond to the maximum expected value of R_s.

(6) The design would have proceeded in the same manner if $\overline{AM}$ and $\overline{ACN}$ represented the expected "worst" case extremities in the load characteristics.

(7) The semi-graphical analysis lends itself to a more comprehensive picture of the static circuit operation; can be used to attack non-linear threshold characteristics (for example if one attempts to design at such low base currents that one is near the "breakpoint"); and illustrates the effect on power dissipation if certain parameters are varied.

The Minimum Base Current and Transistor Grounded - Emitter Current Gain.

In the previous section, the graphical design, which was considered, assumed an arbitrary minimum value of base current and assumed that the "on" transistor was saturated. As might be expected the choice of an actual minimum base current is a function of transistor parameters.

Consider an n_i input and n_o output nor circuit with the "source off" currents as shown in Figure 7a. It is seen that:

$$I_{sf} = n_i I_{co}' + I_w + n_o \underline{I_{bn}}$$

where:

I_{co}' = the "off" transistor collector current

n_i = the number of transistor collectors connected to the common source resistor

I_w = the total "waste" current as defined om section 2a

n_o = the number of transistor bases being driven by the signal source

$\underline{I_{bn}}$ = the minimum acceptable steady-state "on" base current

The same circuit in the "source on" condition has currents shown in Figure 7b. Although all n_i transistors could conceivably be on, any one of them must be capable of supplying the required collector current which is equal to $I_{sn} + n_o I_{co}'$. Let us assume that the saturation voltage of the one on transistor is appreciably less than E_s (thereby qualifying approximately as a "perfect" short circuit).

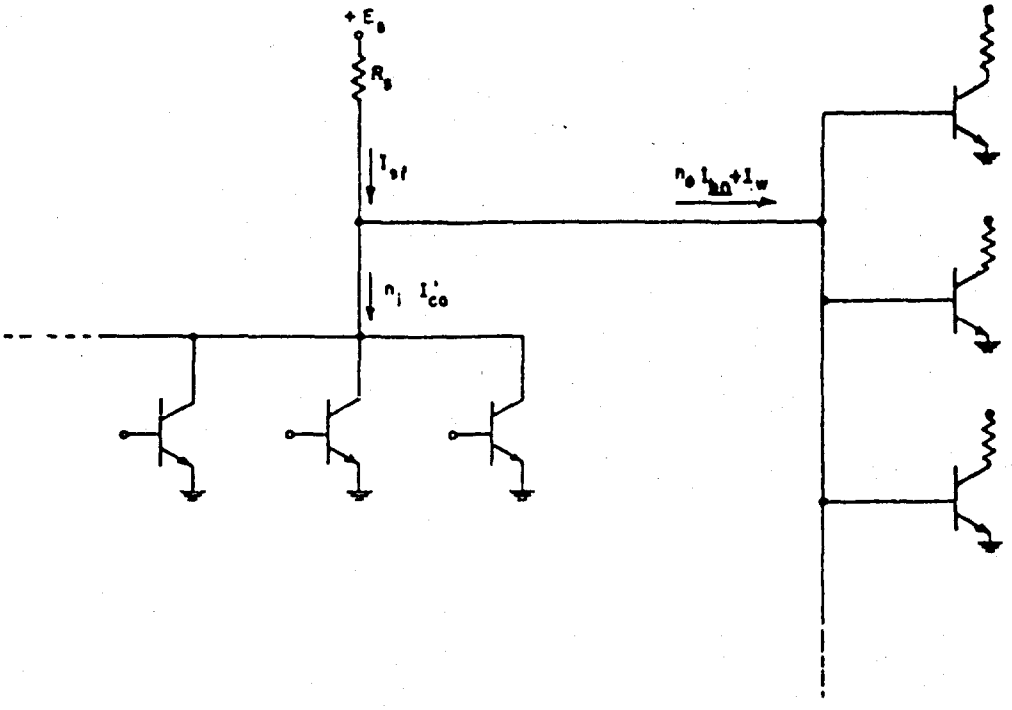


Figure 7a. DCTL "Source-off" Condition (Static)

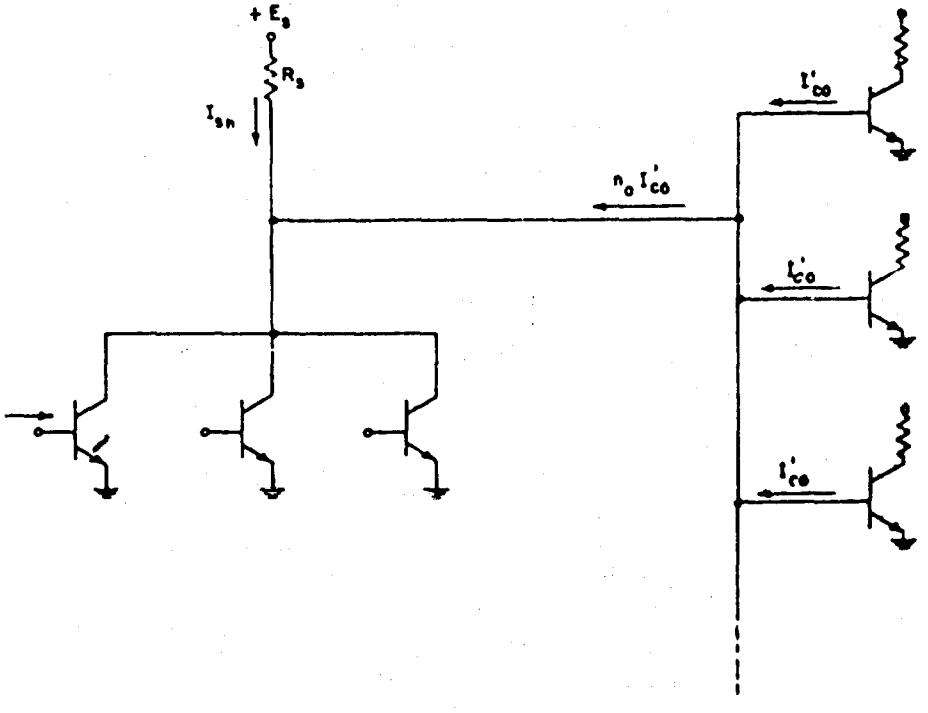


Figure 7b.. DCTL "Source-on" Condition (Static)

Assuming that the Bi-State Nominal Design has been applied to the design of E_s and R_s, I_{sn} must be equal to twice I_{sf}. In order for the "on" transistor to be in saturation, therefore:

$$\beta \underline{I_{bn}} > I_{sn} + n_o I_{co}'$$

but

$$I_{sn} = 2 I_{sf}$$

and

$$I_{sf} = n_i I_{co}' + I_w + n_o \underline{I_{bn}}$$

$$\therefore \quad \beta \underline{I_{bn}} > 2 \left\{ n_i I_{co}' + I_w + n_o \underline{I_{bn}} \right\} + n_o I_{co}'$$

or

$$\underline{I_{bn}} > \frac{(2 n_i + n_o) I_{co}' + 2 I_w}{\beta - 2n_o}$$

where:

β = the minimum expected common emitter current gain of the transistor.

This equation for $\underline{I_{bn}}$ illustrates several very interesting facts. For one thing, the common-emitter current gain must be greater than twice the number of loads being driven. One would, of course, expect the required β to be at least equal to n_o. The factor of two is a direct result of the Bi-State Nominal design. Essentially the price for minimizing the source power dissipation is cutting in half the effective minimum current gain of the transistor. The equation also shows that for values of β much greater than 2 n_o, the current $\underline{I_{bn}}$, at least under static conditions can be made arbitrarily small with increasing β. It is also obvious that even for moderate values of current gain, the $\underline{I_{bn}}$ can be made very small by decreasing I_{co}' and I_w. This is the most favorable approach since as I_{co}' and I_w approach zero, both $\underline{I_{bn}}$ and the total circuit power can also be made to approach zero under static conditions. Instead if $\underline{I_{bn}}$ is made very small just by using high current gain transistors, the static "source on" power dissipation P will approach the value:

$$P = 4(n_i I_{co}' + I_w)(E_{bp\ max})$$

In the design, the minimum expected transistor current gain $\underline{\beta}$ multiplied by the minimum acceptable base current $\underline{I_{bn}}$, must be greater than or equal to the maximum necessary "source on" collector current $\underline{I_c}$, i.e.

$$\underline{\beta}\ \underline{I_{bn}} \geq \underline{I_c}$$

But the maximum necessary "source on" collector current must be greater than or equal to twice the "source off" current requirement plus the number of outputs times the "off" transistor current, i.e.

$$\underline{I_c} \geq 2\left[n_i I_{co}' + I_w + n_o\,\underline{I_{bn}} + \frac{n_o Q}{t}\right] + n_o I_{co}'$$

where

n_i = the number of transistor collectors connected to the common source resistor.

I_w = the total waste current (defined on pages 21 and 23).

n_o = the number of transistor bases being driven by the signal source.

$\underline{I_{bn}}$ = the minimum acceptable steady state "on" base current.

I_{co}' = the "off" transistor collector current.

Q = the total transient charge required by each transistor base and associated capacitance.

t = the switching time.

But from the first equation:

$$\frac{I_c}{\underline{\beta}} \leq \underline{I_{bn}}$$

$$\therefore \underline{I_c} \geq 2 \left[n_i I_{co}' + I_w + n_o \frac{I_c}{\underline{\beta}} + n_o \frac{\varrho}{t} \right] + n_o I_{co}'$$

$$\therefore \underline{I_c} \geq \frac{2\underline{\beta}}{\underline{\beta} - 2n_o} \left[n_o I_{co}' + I_w + n_o \left(\frac{\varrho}{t} + \frac{I_{co}'}{2} \right) \right]$$

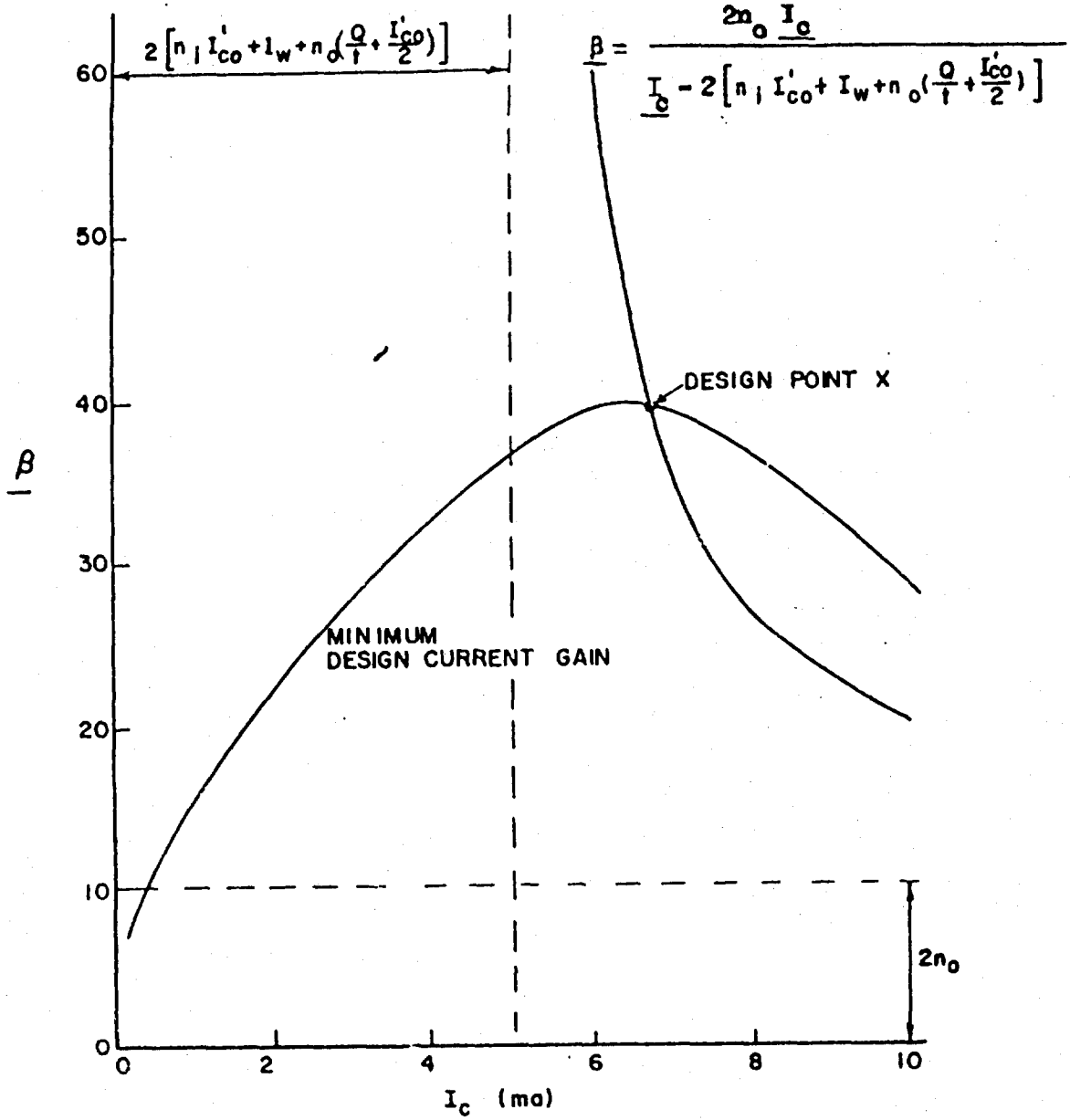
$$\therefore \underline{\beta} \geq \frac{2n_o \underline{I_c}}{\underline{I_c} - 2 \left[n_i I_{co}' + I_w + n_o \left(\frac{\varrho}{t} + \frac{I_{co}'}{2} \right) \right]}$$

The equality portion of the above relationship is plotted in Figure 8. Also plotted in the curve is a typical assumed curve showing the variation of minimum expected current gain as a function collector current. The intersection of the two curves represents the minimum acceptable collector current. This allows the minimum acceptable base current to be established on the basis of the minimum expected current gain. The minimum acceptable base current is simply given by:

$$\underline{I_{bn}} = \frac{I_{cX}}{\beta_X}$$

where "X" denotes the respective values for the intersection of the two curves.

It is interesting to note the two lines to which the $\underline{\beta}$ curve is asymptotic. The line parallel to the collector current axis is a pure function of the fan-out. The other line is a function of the leakage currents, the waste currents, and the transient currents. Thus, if in



$$I_{bn} \geq \frac{I_{cx}}{\beta_x}$$

Figure 8. Graphical Determination of I_{bn} for the DCTL-NOR

a particular situation, the two curves should not intersect (indicating an impossible situation), it can be easily observed to what degree one of the factors must be decreased in order to enable an intersection and thereby a realizable solution.

This outlined technique is also interesting in that any arbitrary non-linear β versus I_c characteristic can be easily and exactly handled.

For simplicity of future notation, a new variable will be defined:

$$\psi = n_i I'_{co} + I_w + n_o \left[\frac{Q}{t} + \frac{I'_{co}}{2} \right]$$

Therefore, the design inequality becomes:

$$\beta \geq \frac{2 n_o \underline{I_c}}{\underline{I_c} - 2 \psi}$$

and the equality curve is asymptotic to vertical line at $I_c = 2 \psi$.

b. Establishing Operational Property "Trade-offs" for an Example.

In this section, the design techniques outlined in the previous section are applied to ascertain some of the operational property "trade-offs" for the DCTL-NOR circuit.

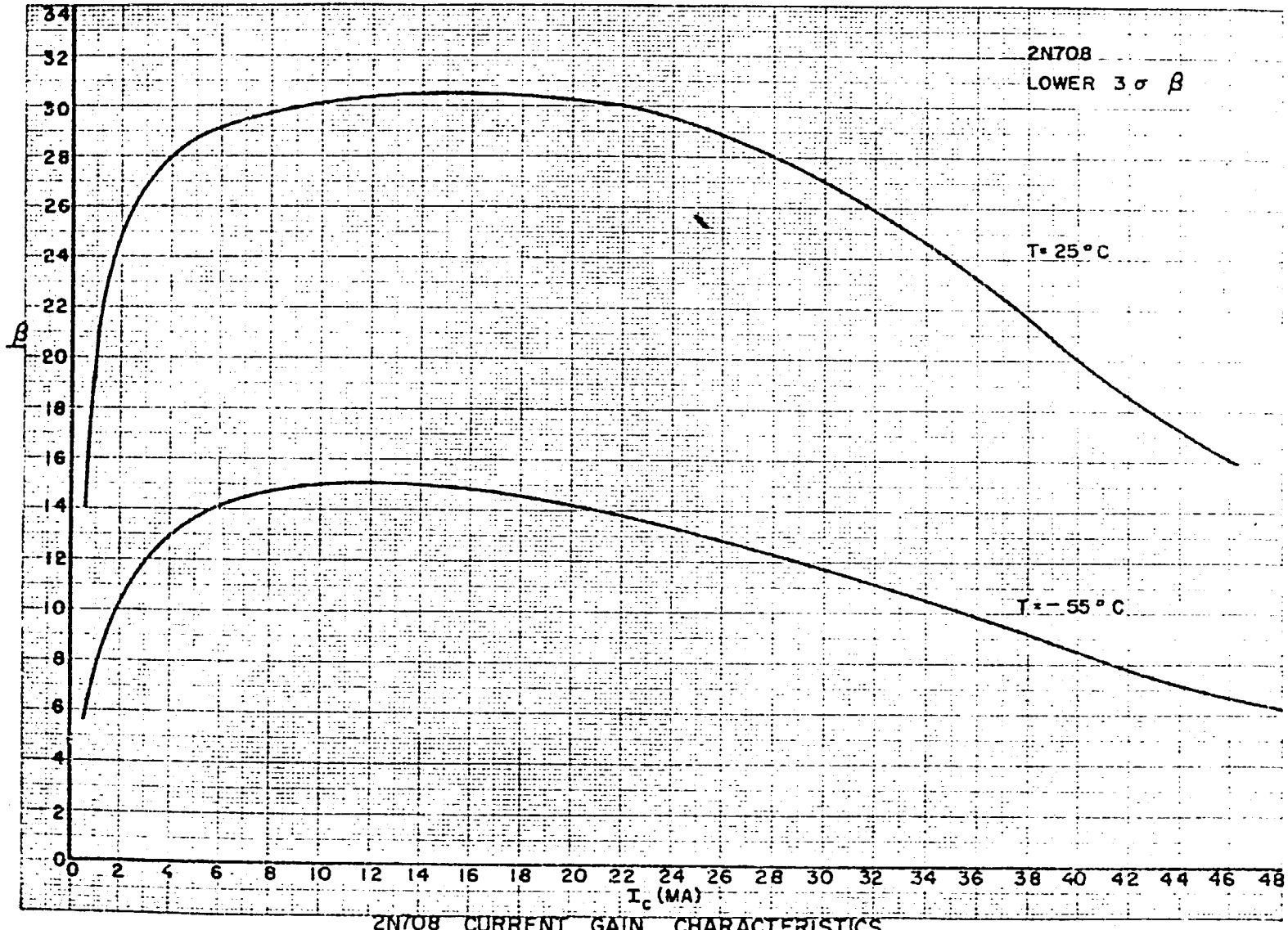
The transistor type selected for this example was the 2N708. The immediately pertinent parameter information is shown in Figures 9 and 10. At any temperature, the common emitter current gain of a transistor type is characterized by a certain "spread" or distribution. The two curves in Figure 9 show the lower 3σ limit of the 2N708 at 25°C and -55°C, respectively. This information was derived from the manufacturer's data sheet.

Figure 10 shows a family of curves with the I_b vs. V_{be} axes The two lines associated with the 80% indicate that the I_b vs. V_{be} characteristic of a random transistor has a probability of 0.8 that it will fall between the lines. Similar statements concerning a probability of 0.90, 0.96, 0.98, and 0.99 for the lines associated with the other percentages. It will be noted that the same lower limit is common to all the pairs. This information was derived from a group of over 200 transistors. While not necessarily representing a typical sample, it was the most complete information available. Unfortunately, the curves do not extend to values of base current less than one milliampere. It would have been extremely desirable to have the more elaborate information in establishing designs and trade-offs at very low power levels.

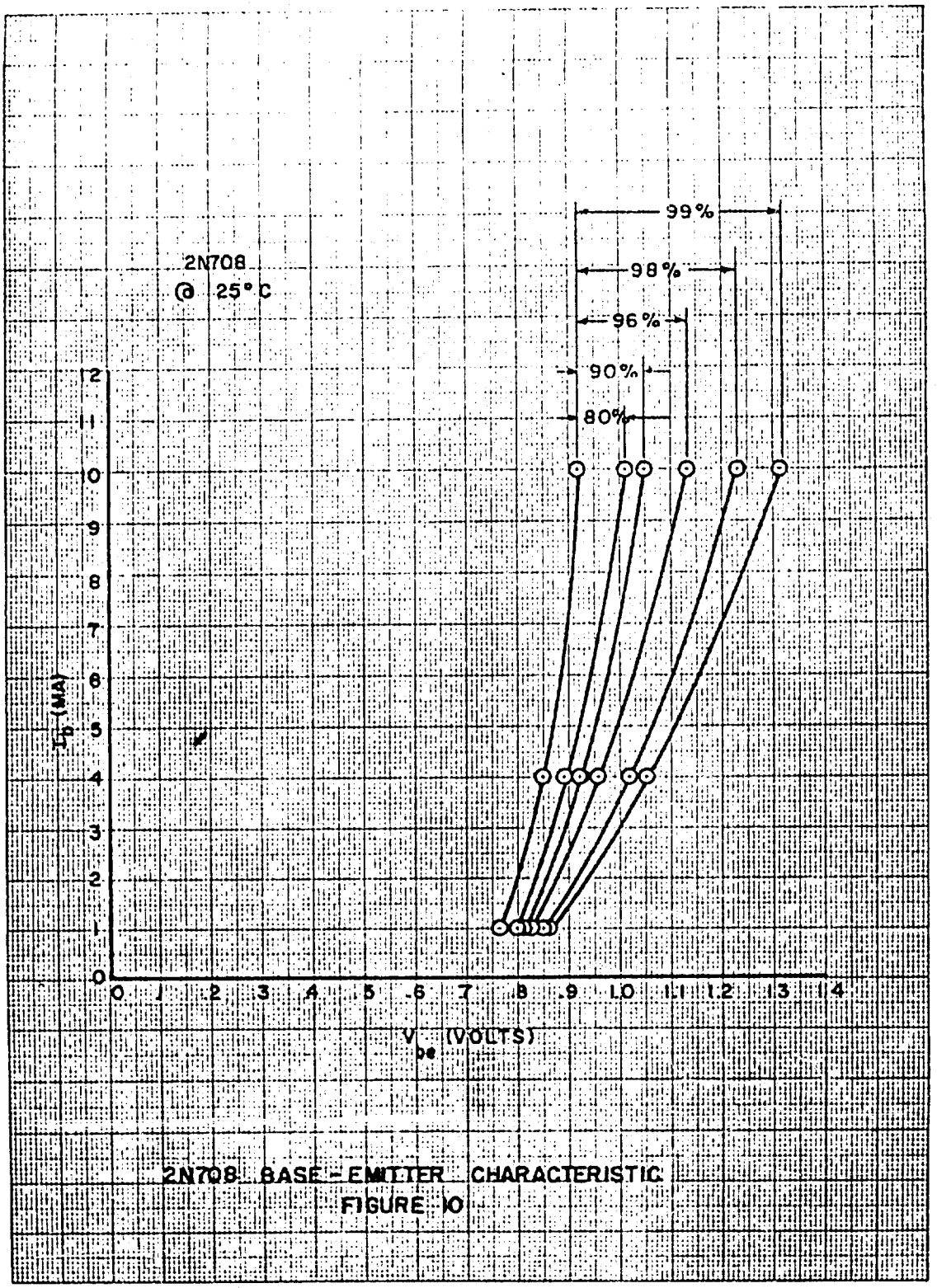
Figure 11 showing the incremental waste current for the 2N708 was directly derived from the information in Figure 10. The dashed lines show an approximate extrapolation of the information for values of base current less than one milliampere.

In section A-4a of this report, a variable, Ψ, was defined as:

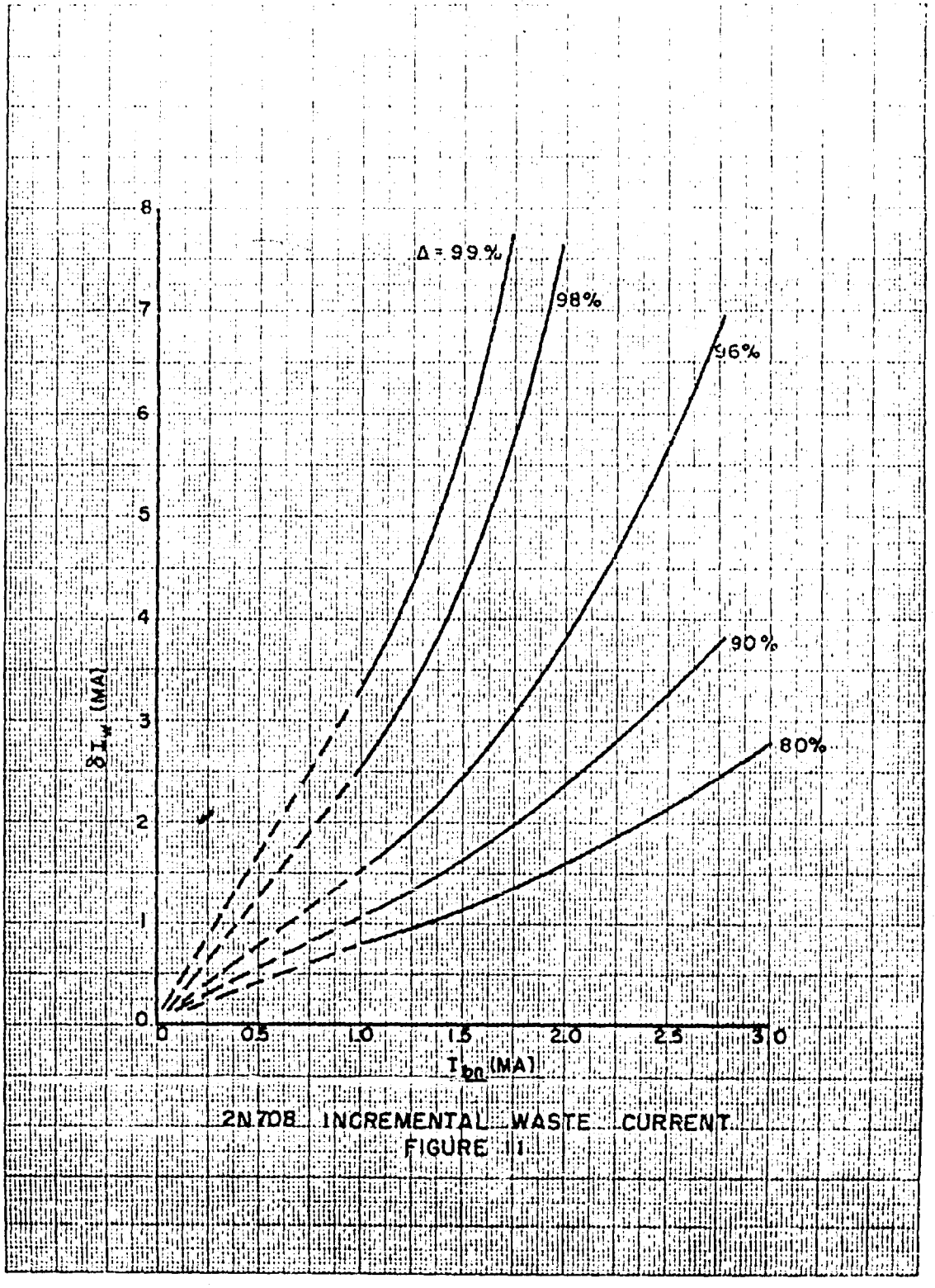
$$\Psi = n_i \dot{I}_{co} + \dot{I}w + n_o \left[\frac{Q}{t} + \frac{\dot{I}_{co}}{2} \right]$$



2N708 CURRENT GAIN CHARACTERISTICS
FIGURE 9



2N708 BASE - EMITTER CHARACTERISTIC
FIGURE 10



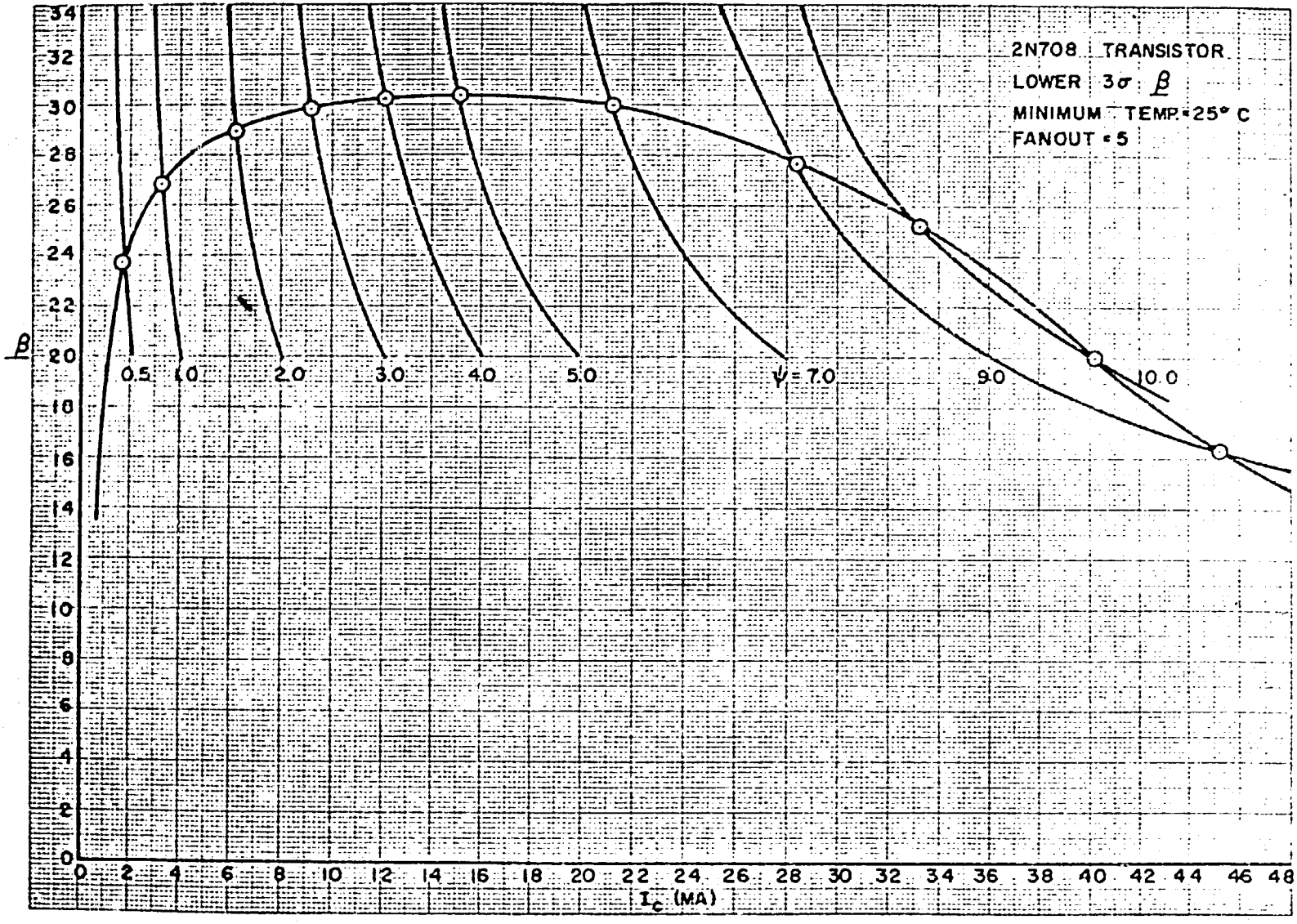
2N708 INCREMENTAL WASTE CURRENT
FIGURE 11

It was further shown that there is a minimum acceptable common emitter current gain, $\underline{\beta}$, which is given by:

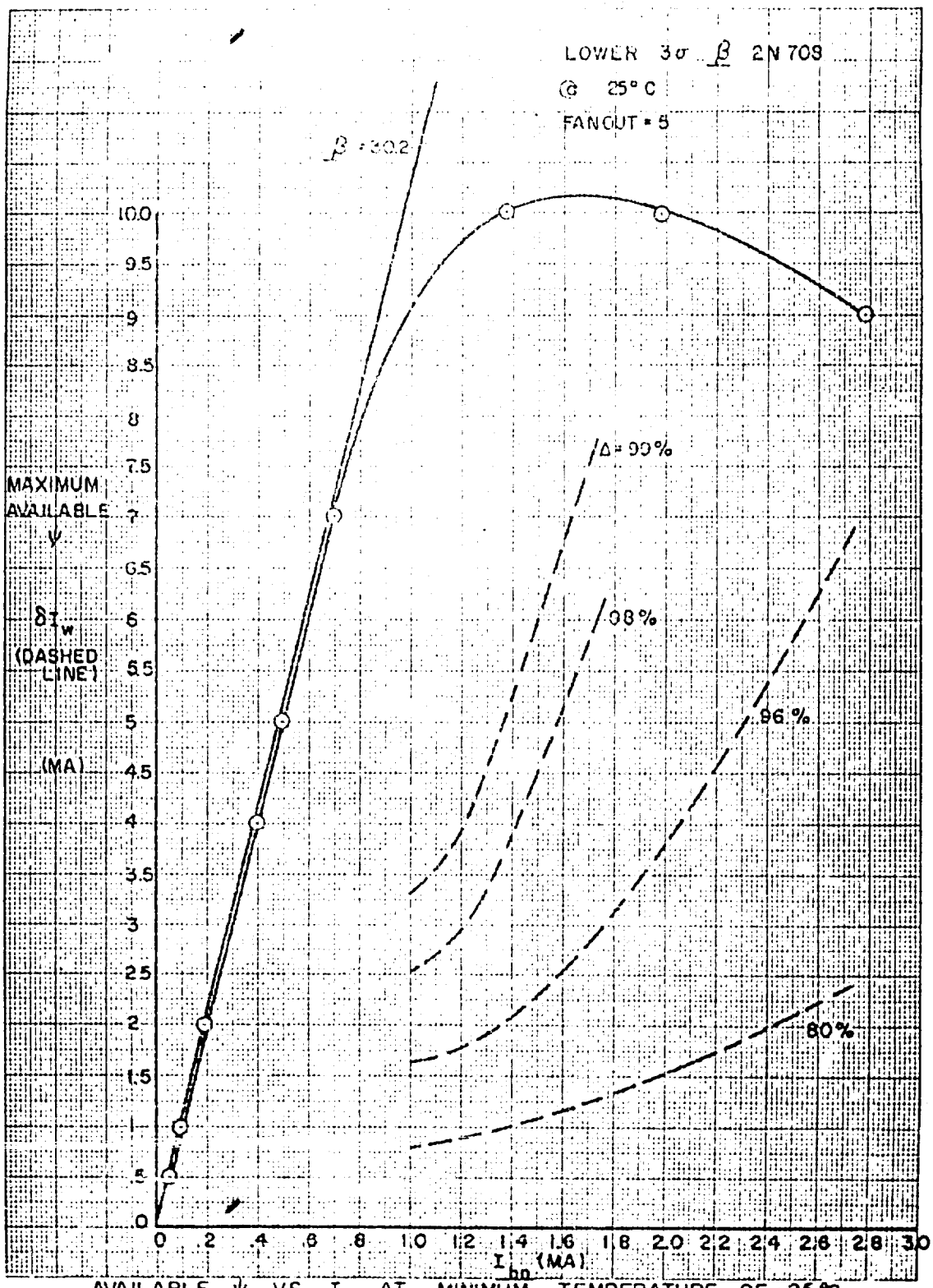
$$\underline{\beta} = \frac{2n_o I_c}{I_c - 2\Psi}$$

If the fanout factor is fixed arbitrarily, the intersection of the above required equation with the minimum expected β vs. I_c characteristic automatically fixes the value of $\underline{\beta}$, I_c, and $\underline{I_{bn}}$ for any particular value of Ψ.

An example of this is shown in Figure 12. On top of the graph of the variation of the lower 3σ common emitter current gain of a 2N708 at 25°C is superimposed the plots of the above equation for a fixed fanout of 5 and for Ψ equal to 0.5, 1.0, 2.0, 3.0, 4.0, 5.0, 7.0, 9.0 and 10.0. Dividing the minimum acceptable collector current by the $\underline{\beta}$ at each intersecting point establishes a certain minimum acceptable base current, $\underline{I_{bn}}$. The result of such computations at each intersecting point yields the solid curved line in Figure 13. This solid curved line shows a very interesting effect! As the minimum base current, $\underline{I_{bn}}$ is increased, the available Ψ increases to a point and then <u>decreases</u> for further increasing $\underline{I_{bn}}$. Ψ can be thought of as a net available current which can be divided amongst leakage current, waste current, and transient overdrive current. This maximum in the Ψ versus $\underline{I_{bn}}$ curve is due to the fact that the transistor gain decreases with sufficiently high collector current. A transistor gain which remained constant at 30.2 at all higher value of collector current would result in the line tangent to the solid curve. The dashed lines of Figure 13 are a duplicate of Figure 11. The two sets of curves are superimposed to show that a substantial portion of the available Ψ may be used up by the waste current thereby substantially decreasing potential speed due to lack of transient overdrive current. The superposition also shows that as one **increases the probability that sufficient base current is being supplied, one decreases the current available for switching speed and leakage current.**



SUPERPOSITION OF β CHARACTERISTIC AND DESIGN EQUATION
AT MINIMUM TEMPERATURE OF 25°C
FIGURE 12



AVAILABLE ψ VS. I_{bn} AT MINIMUM TEMPERATURE OF 25°C

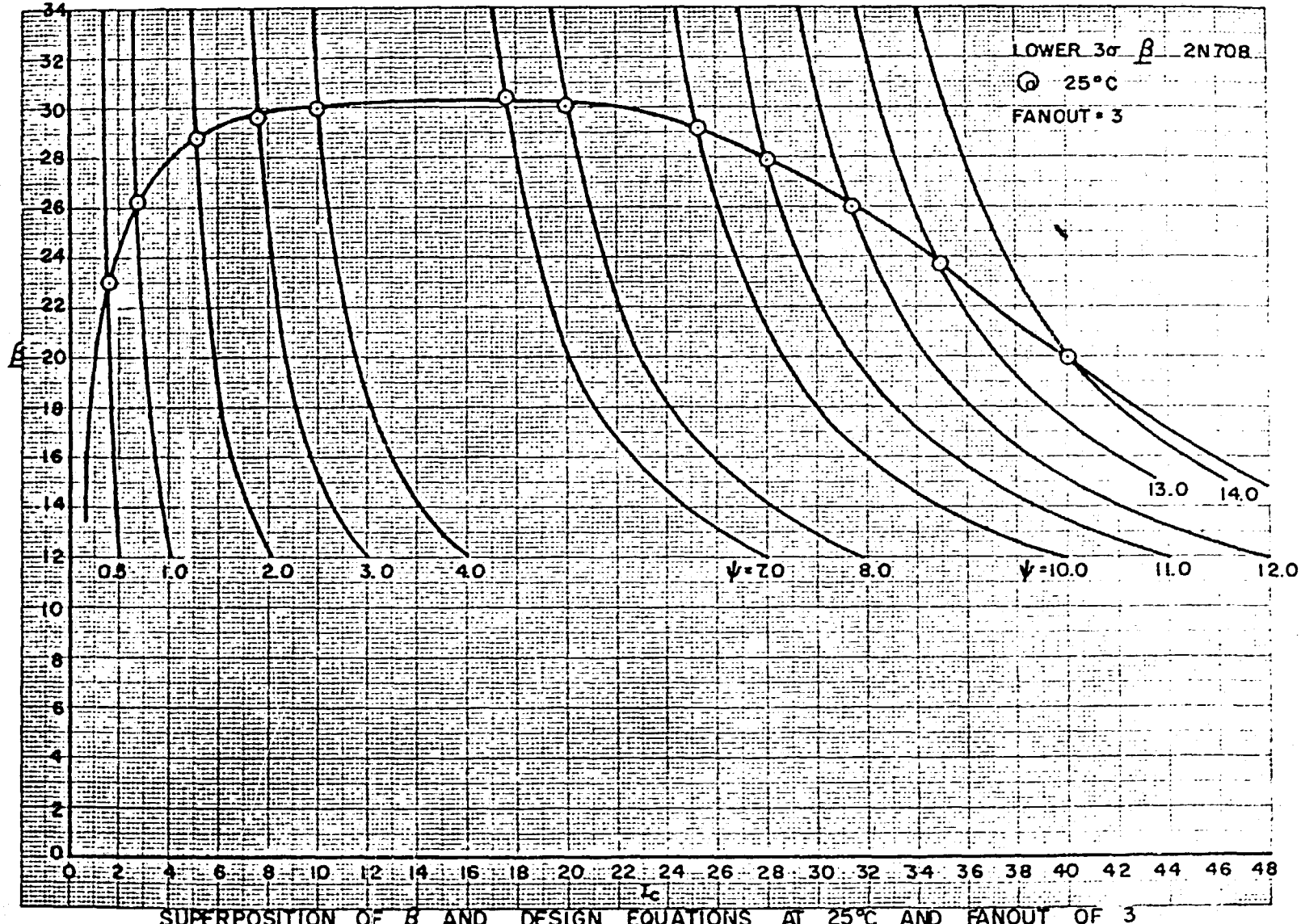
FIGURE 13

In Figure 14, a superposition solution is carried out the same as in Figure 12 except that the fanout is changed from 5 to 3. The resulting available ψ versus $\underline{I_{on}}$ is shown in Figure 15, along with a reproduction of Figure 13.

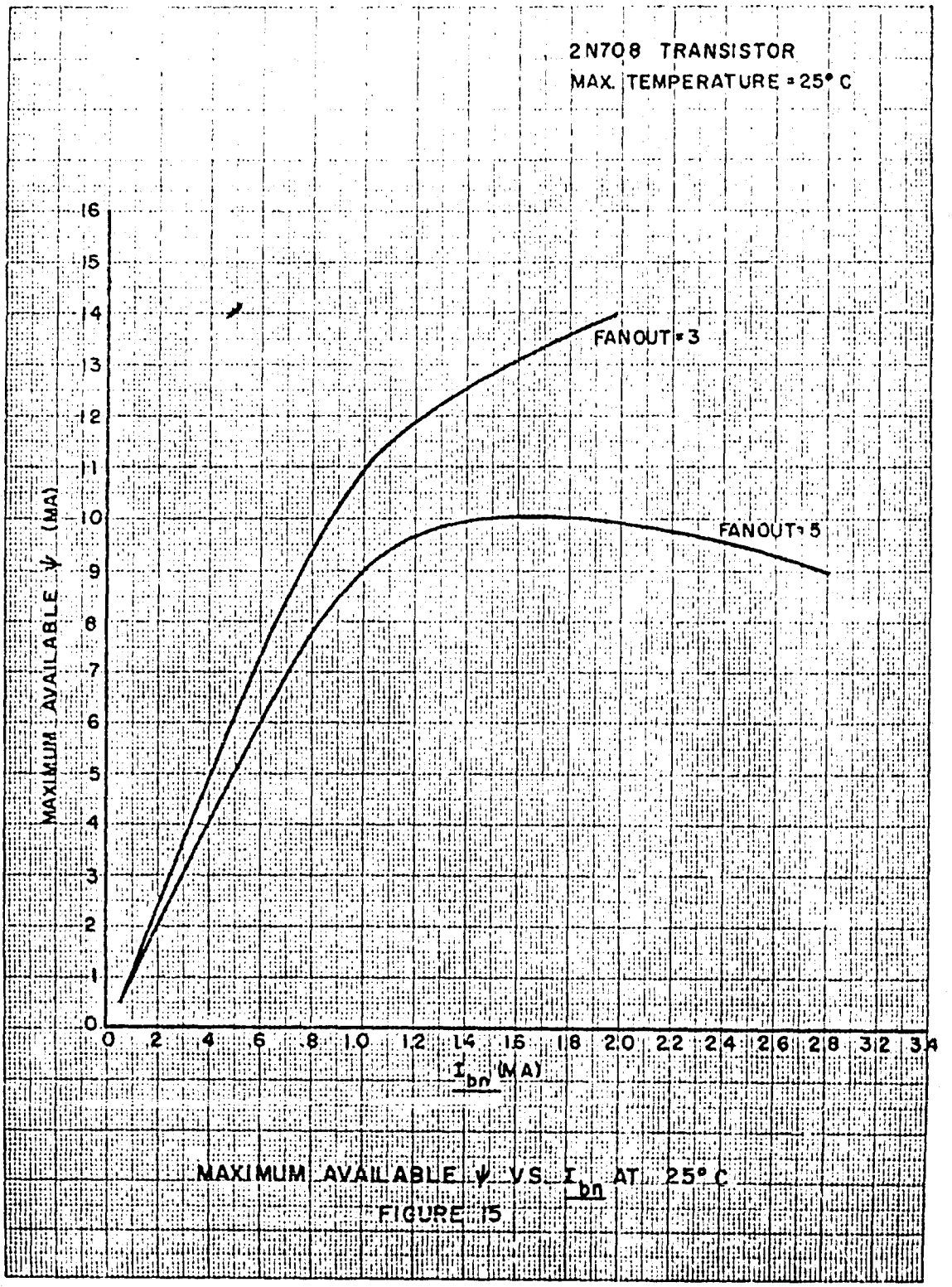
The intersection points in Figures 12 and 14 can also be used to derive the available ψ versus minimized power curve as shown in Figure 16. The computations proceed as follows: with each intersection point in Figures 12 and 14 is associated a particular $\underline{\beta}$, I_c, $\underline{I_{bn}}$ and ψ. With each $\underline{I_{bn}}$, there is associated a particular $\overline{V_{be}}$ from Figure 10, for a given degree of confidence. (The curves of Figure 16 are derived for 99%.) Applying the Bi-State Nominal Design technique establishes a minimum acceptable value for E_s, the supply voltage. The product of E_s and I_s represents the minimized power dissipation for the particular point. Each value of minimized power is associated with a certain value of ψ which is plotted in Figure 16.

If it is temporarily assumed that it is possible to decrease (perhaps by selection) the leakage current and waste current to values which are small with respect to the transient switching current, the question would arise as to the trade-off between maximum frequency of operation and minimized power dissipation. In other words, it is temporarily assumed that all the available ψ is used for maximizing the frequency of operation and it is not necessary to use any appreciable portion to overcome leakage and waste currents. The solid lines in Figure 21 show such a trade-off for a minimum temperature of 25°C; a 10% of the period switching time; and a per load unit charge of 50 picocoulombs. The per load unit charge is the charge necessary to sufficiently supply the effective per load capacitance. The effective per load capacitance includes the effective capacitance of the transistor input including storage and switching effects along with the packaging and wiring stray capacitance.

The results in Figure 21 are based on zero waste current. This is equivalent to using a 0% confidence spread or distribution as per

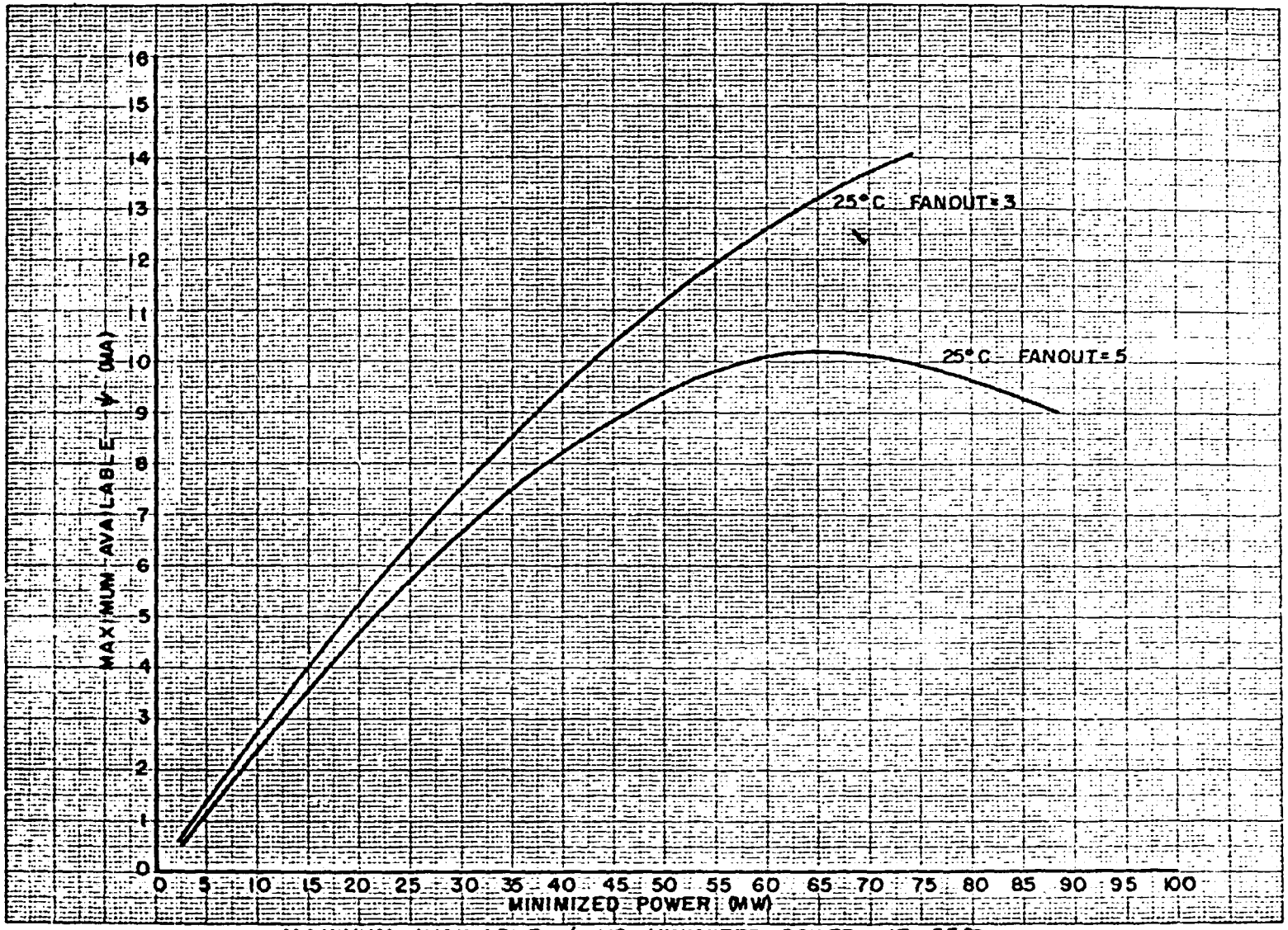


SUPERPOSITION OF β AND DESIGN EQUATIONS AT 25°C AND FANOUT OF 3
FIGURE 14



MAXIMUM AVAILABLE ψ V.S. I_{bn} AT 25° C

FIGURE 15



MAXIMUM AVAILABLE ψ VS. MINIMIZED POWER AT 25°C
FIGURE 16

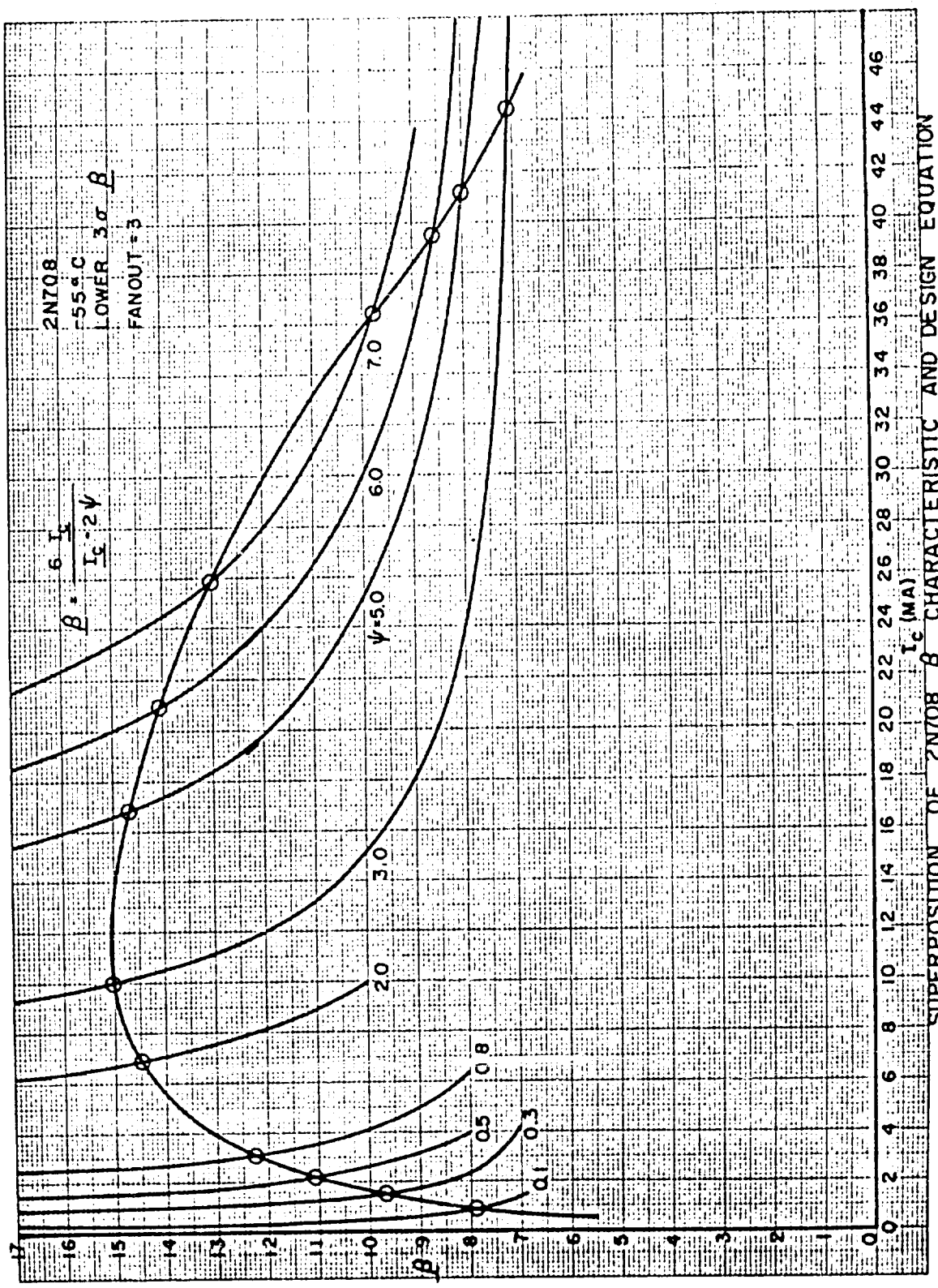
Figure 10. Introducing higher confidence limits increases the waste current as shown in Figure 11. In Figure 11, for a particular value of I_{bn}, the waste current increases with higher confidence limits.

In Figure 23, the "fanout = 3" solid line of Figure 21 has been recopied and labeled 0%. The 80% solid line in Figure 23 shows the effect of introducing the 80% confidence limit waste current into the solution. Likewise, the solid 99% line shows the affect of introducing the 99% confidence limit waste current into the solution. As might be expected, as more and more available Ψ is allocated to furnish waste current, the maximum realizeable frequency of operation decreases for the same circuit power dissipation.

It should be noted that whereas Figure 16 is relatively general in nature, Figures 21 and 23 are relatively more restricted in that a unit charge of 50 picocoulombs has been somewhat arbitrarily selected. If packaging and wiring restrictions in a particular situation should warrant a different unit charge, new curves would need to be calculated.

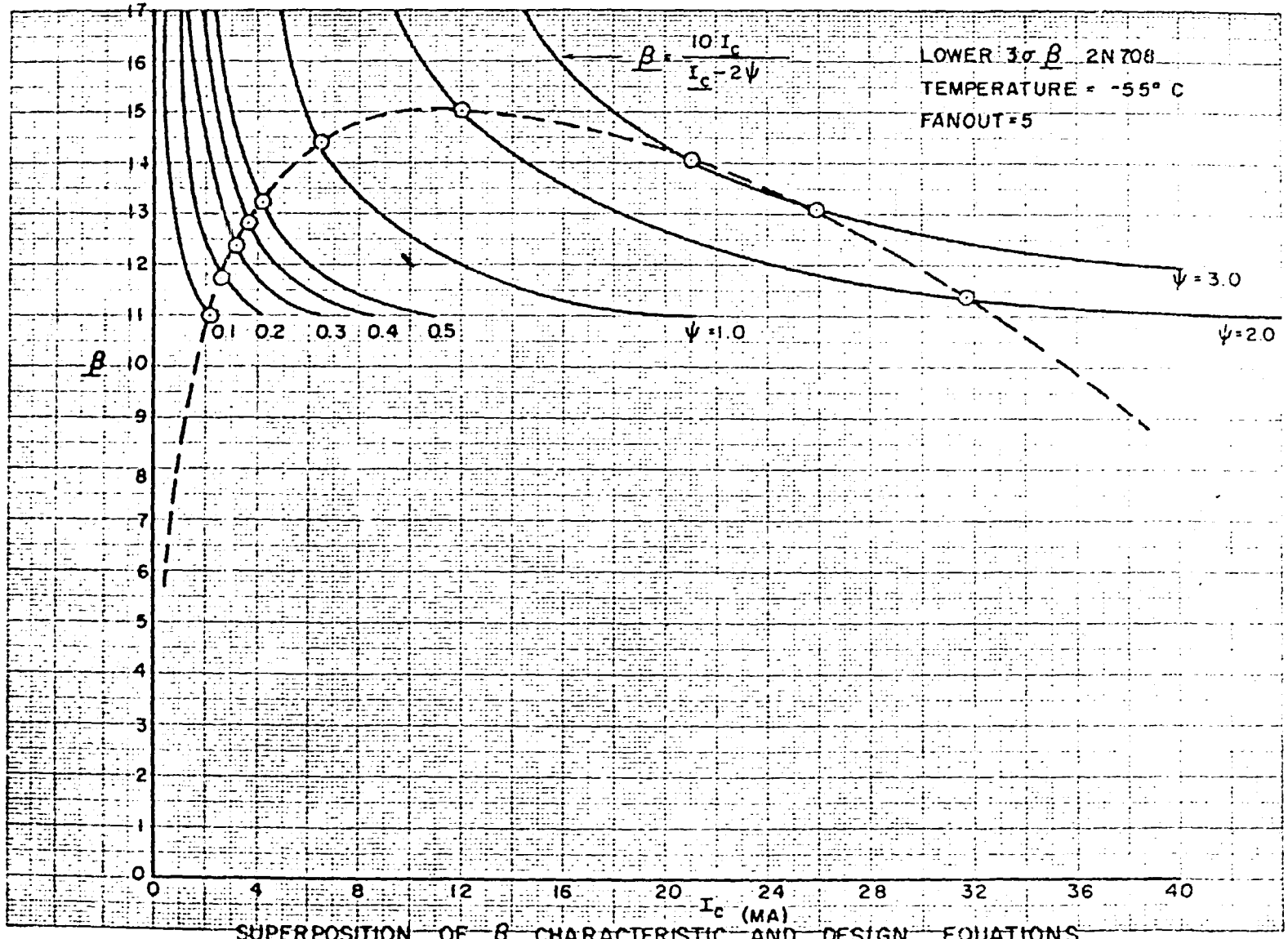
All of the above results have been based on a minimum system temperature of 25°C. As shown in Figure 9, there is a considerable drop in β with decreased temperature. The question arises as to the effect on the previously generated "trade-off" curves if the minimum system temperature is decreased to -55°C. The superposition solution shown in Figure 17 is related to Figure 14 except for the use of the -55°C β versus I_c characteristic instead of the +25°C characteristic. Likewise, Figure 18 is related to Figure 12. The available Ψ versus I_{bn} curves derived from the superposition solutions of Figures 17 and 18 are shown in Figure 19. Likewise, the available Ψ versus minimized power curves are shown in Figure 20.

Comparing Figures 16 and 20, the price of operating at -55°C instead of +25°C in terms of available Ψ for a given minimized power is substantial.

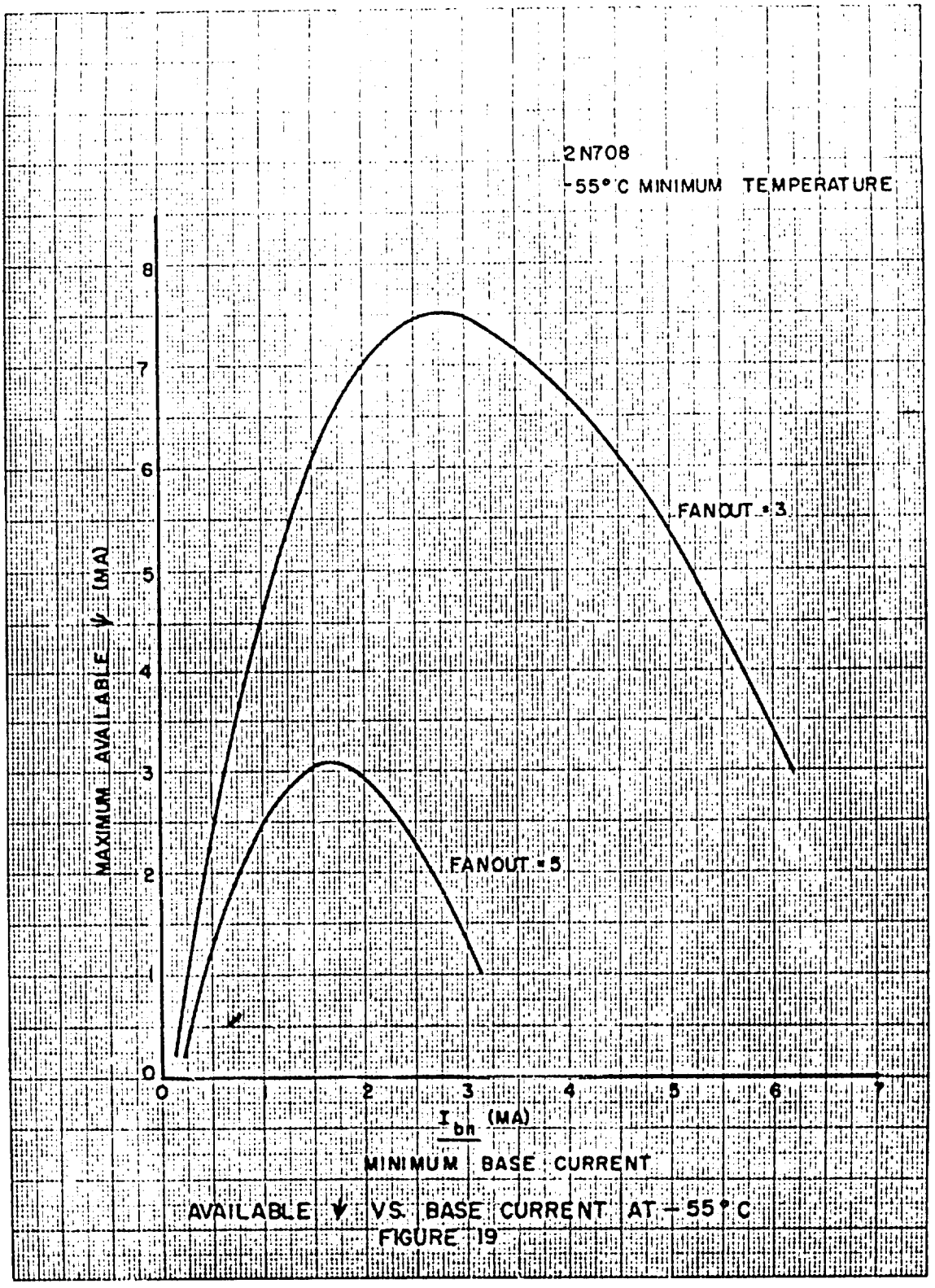


SUPERPOSITION OF 2N708 β CHARACTERISTIC AND DESIGN EQUATION

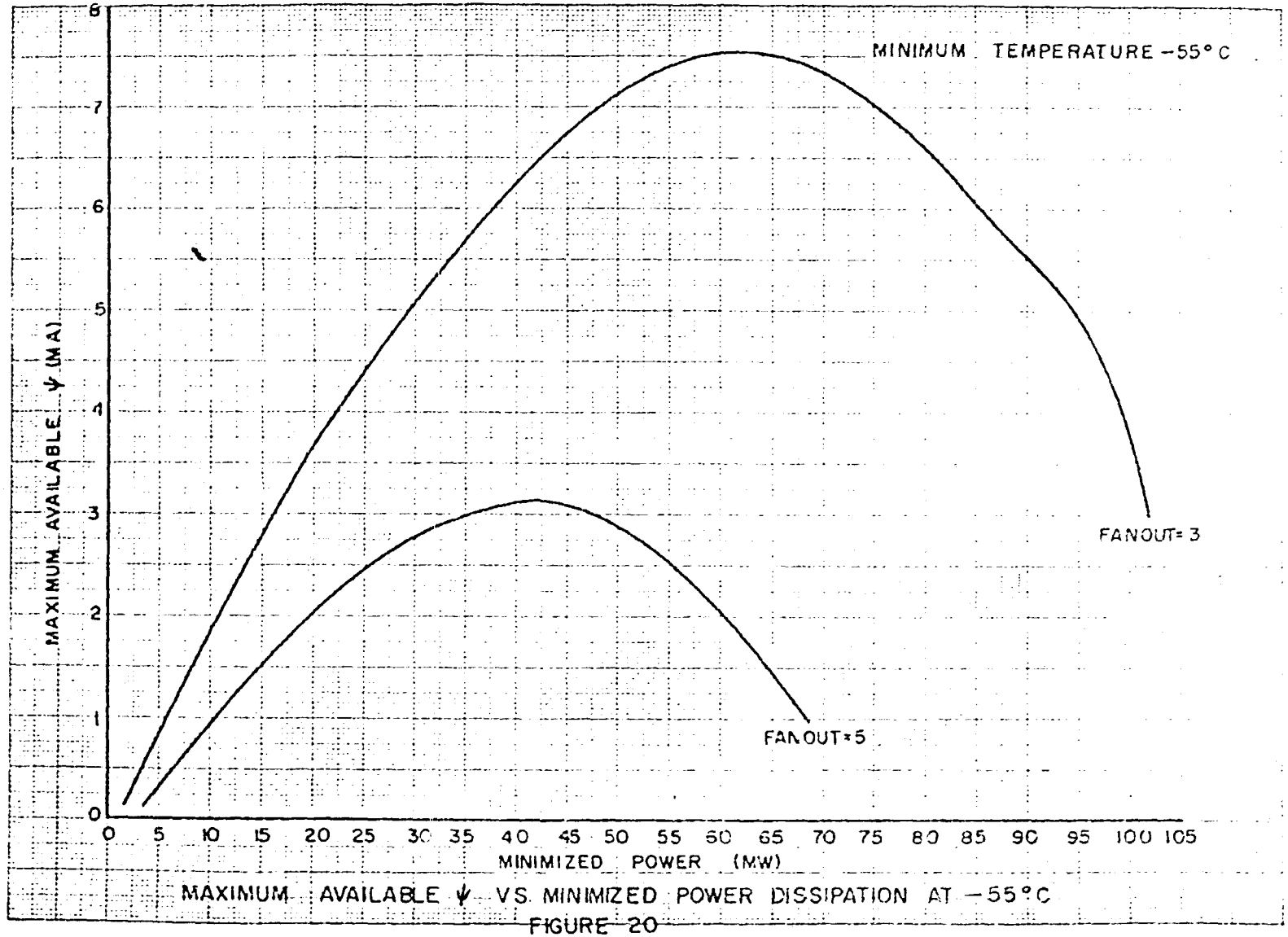
FIGURE 17



SUPERPOSITION OF β CHARACTERISTIC AND DESIGN EQUATIONS
FIGURE 18



AVAILABLE V VS. BASE CURRENT AT −55° C
FIGURE 19



MAXIMUM AVAILABLE ψ VS. MINIMIZED POWER DISSIPATION AT -55°C

FIGURE 20

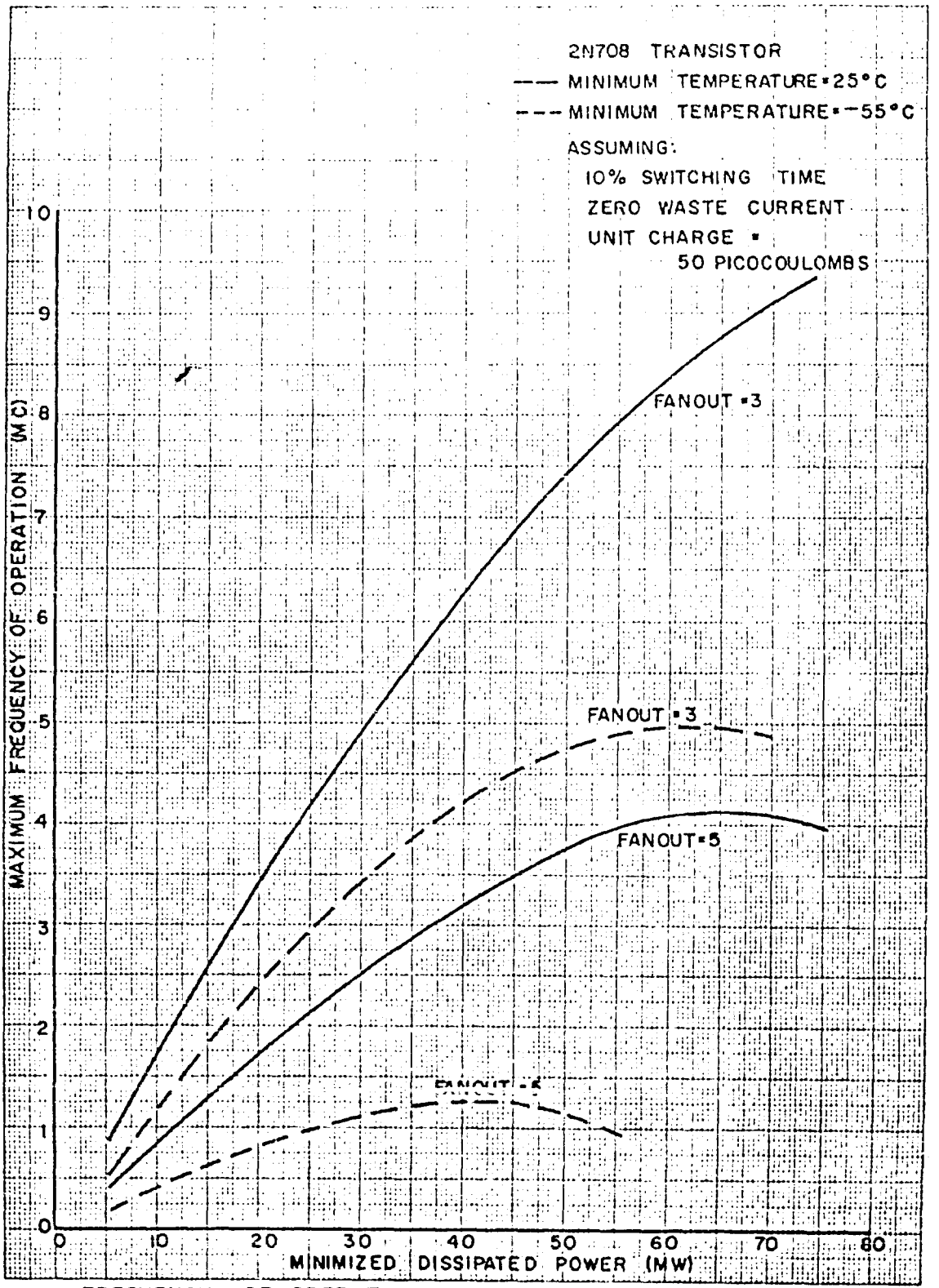
The dashed lines in Figure 21 show the maximum frequency versus minimized power curves for a minimum temperature of -55°C. Comparing the dashed and solid curves in Figure 21, it is evident that there is a substantial power price for equivalent operational properties when designing for -55°C. What is perhaps even more important is the fact that the maximum realizeable maximum frequency of operation is substantially decreased. In other words, it is bad enough to have to pay a higher power price for equivalent operational property performance, but it is extremely unfavorable to be unable to increase the operational properties no matter what the power price one is willing to pay.

Figure 22 shows Frequency versus power curves (Fanout =3; 0% confidence limit on waste current; 25°C) for different values of unit charge. The 50 picocoulomb curve is identical to the 25°C fanout =3 curve of Figure 21. The purpose of Figure 22 is to show the effect of varying circuit effective capacitance and signal amplitude on the performance per unit power.

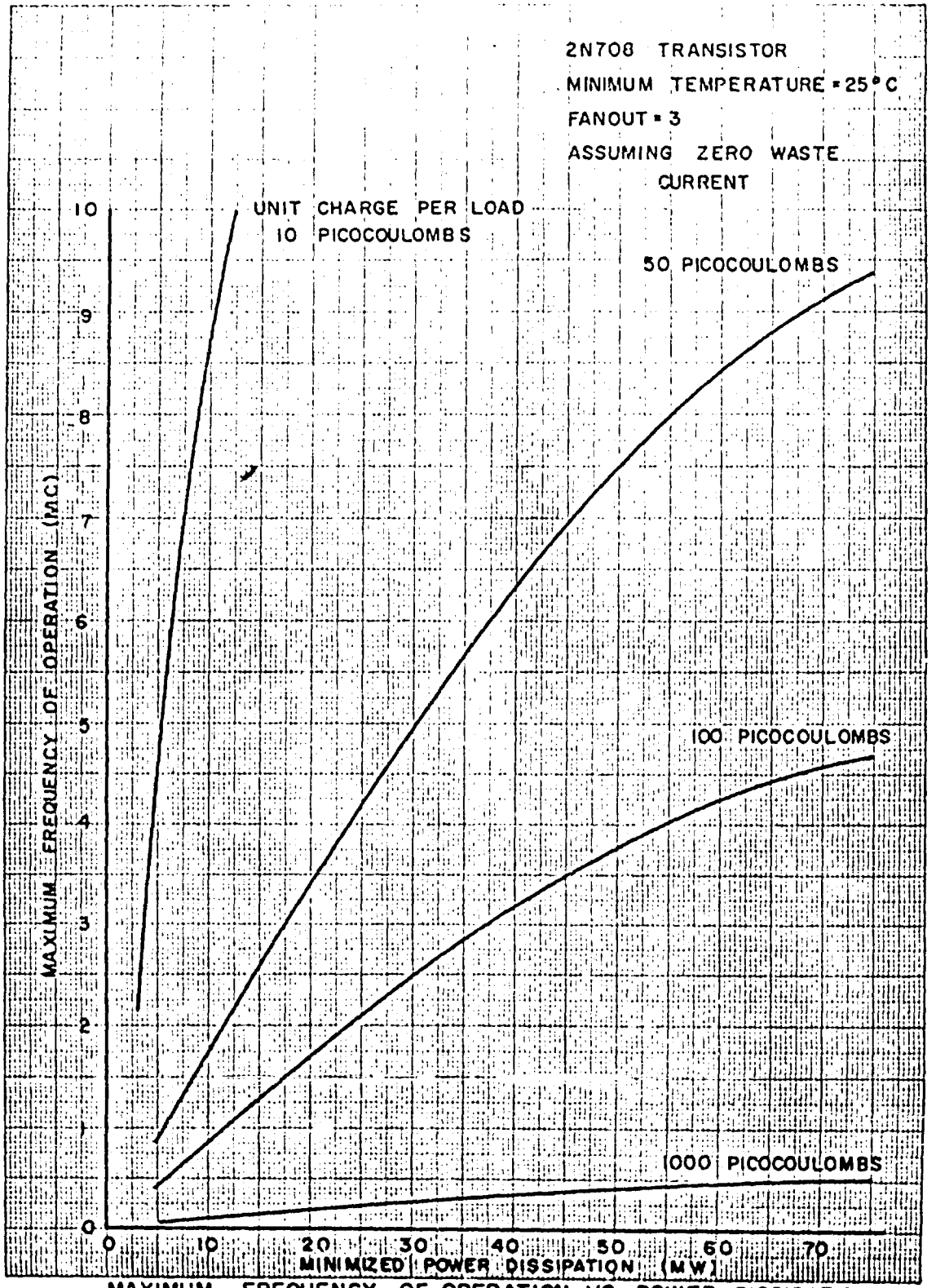
The solid curves of Figure 23 have already been discussed. The dashed lines are the result of lowering the minimum temperature to -55°C. It will be noted that the 99% dashed line is listed as unrealizable. The cause of this was that the total waste current was greater than the available ψ under all operating currents. Therefore, there was no available current to supply leakage and transient overdrive conditions.

It should be reiterated that the example here has been carried out using rather insufficient and not necessarily accurate data concerning the transistors. If optimum circuit design is ever to be realized, it is absolutely necessary that more information be known of the variation of parameters under varying conditions of temperature, radiation level, current, etc.

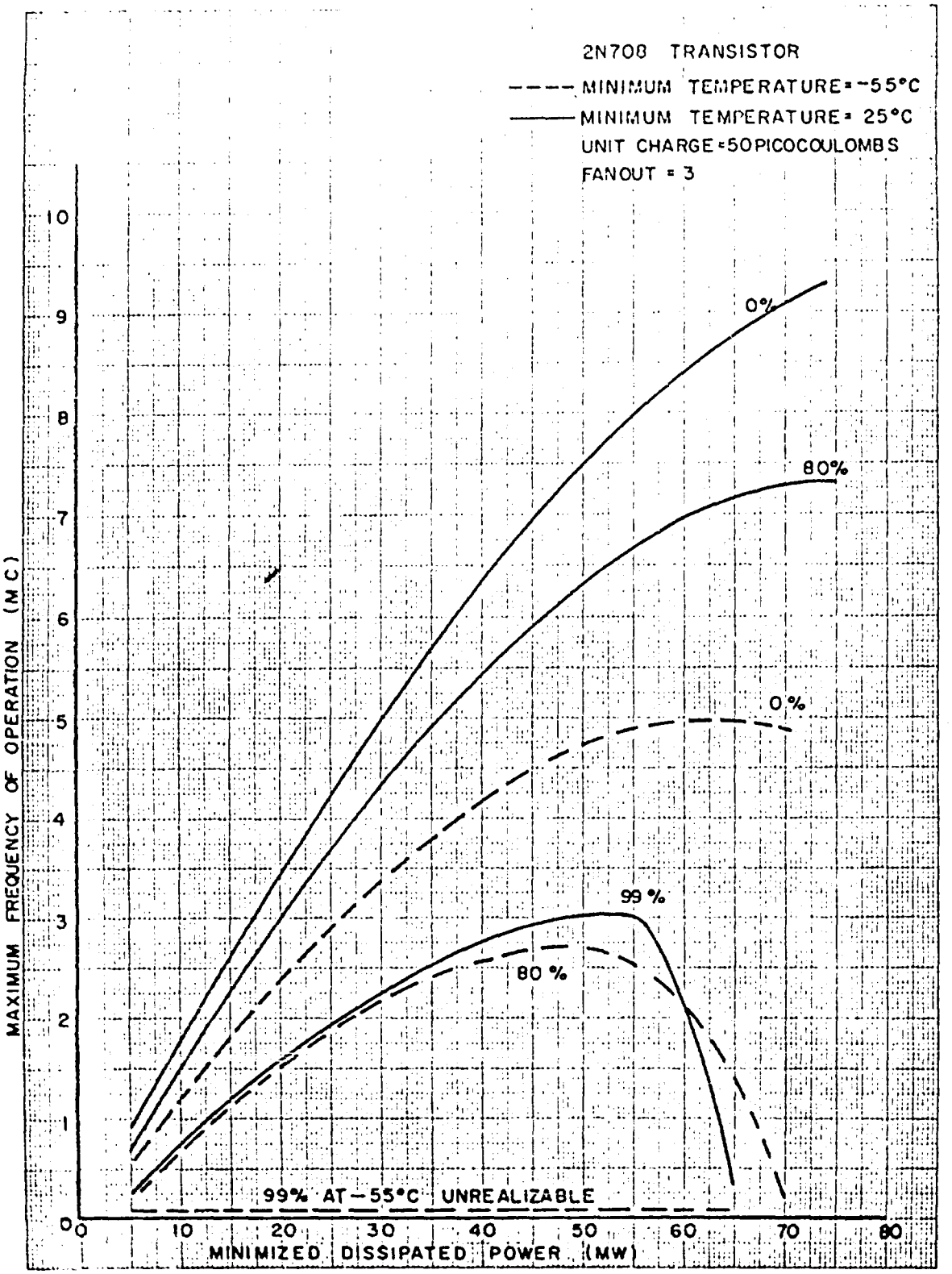
In spite of some question related to data accuracy, this example has illustrated some interesting ideas along with showing approximate numbers. One of these is the idea of an available ψ current which can be allocated for different purposes such as leakage current, waste current, and transient overdrive current. The effect of a decrease in the common-emitter current gain becomes quite drastic as it approaches twice the fanout, n_o.



FREQUENCY OF OPERATION VS. POWER DISSIPATION
FIGURE 21



MAXIMUM FREQUENCY OF OPERATION VS. POWER DISSIPATION
FIGURE 22



FREQUENCY VS. POWER AT DIFFERENT CONFIDENCE LEVELS
FIGURE 23

4. DTL-NOR Circuit Design

a. Some Minimum Power Considerations

The Diode-Transistor Logic circuit shown in Figure 24 is the subject of the present discussion. A qualitative discussion of the function of the various circuit components may be appropriate at this time. The major function of the resistor R_K is to provide a voltage shift in the non-conducting state to compensate for "source" diode and transistor voltage drops such as to insure that the transistor is reliably non-conducting. To provide a proper voltage shift, R_K must conduct current "toward" the transistor base. Since the transistor is "off", the current cannot flow into the transistor. Therefore, a resistor R_B is included to provide a current path. In order to enable the design of a non-conducting base voltage equal to or less than zero, the resistor R_B is returned to a negative supply voltage, E_B. The voltage supply E_D, the resistor R_D, and the series combination of gate diode and previous stage saturated transistor constitute a signal source as directly related to Figure 2-b. The diode-saturated transistor combination replaces the "idealized" single throw switch. The resistor R_L is not a necessary circuit component in most situations. Except where transmission line effects appear (at high frequencies of operation), any function performed by R_L can be done instead by R_D. Therefore, R_L will be assumed removed from the circuit in the present discussion.

Most of the power dissipated by this circuit is concentrated at R_D. In fact, applying the idea of the Bi-State Nominal Design of Section IV-A-3-d, it is known that the minimum "transistor non-conducting" power dissipated in R_D is approximately four times the "transistor conducting" power as seen from the input to R_K.

Let us consider the power dissipated in R_K in the "transistor conducting" state. The current flowing in R_K, in this state, is given by:

$$I_{KON} = I_B + \frac{V_{shift}}{R_K} + \frac{\Delta V_{be}}{R_B} \qquad (23)$$

Best Available Copy

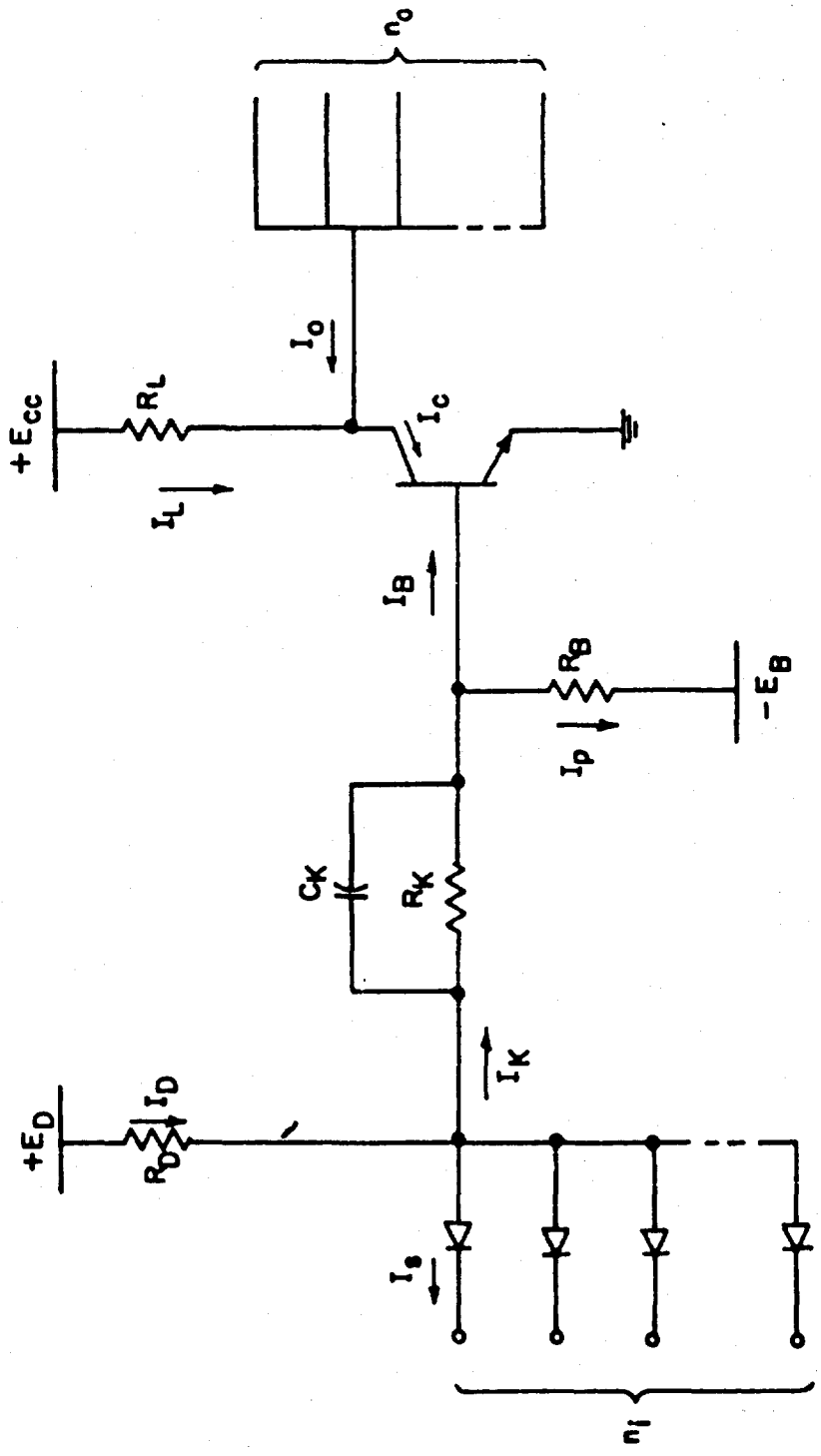


Figure 24. "NAND" Gate

where

I_b = the required base current

V_{shift} = the voltage shift which was designed for the "transistor off" state

ΔV_{be} = the change in base to emitter voltage between the conducting and non-conducting states.

the power dissipated in R_K is then given by:

$$P_K = \left[I_B + \frac{V_{shift}}{R_K} + \frac{\Delta V_{be}}{R_B} \right]^2 R_K \qquad (24)$$

Taking the first derivative with respect to R_K and setting it equal to zero, the value of R_K is found which minimizes the maximum power dissipated in R_K:

$$\frac{dP_K}{dR_K} = \left[I_B + \frac{V_{shift}}{R_K} + \frac{\Delta V_{be}}{R_B} \right]^2 - \frac{2V_{shift}}{R_K} \left[I_B + \frac{V_{shift}}{R_K} + \frac{\Delta V_{be}}{R_B} \right] = 0 \qquad (25)$$

$$\therefore \quad \frac{V_{shift}}{R_K} = I_B + \frac{\Delta V_{be}}{R_B} \qquad (26)$$

and

$$R_K = \frac{V_{shift}}{I_B + \frac{\Delta V_{be}}{R_B}} \qquad (27)$$

It will be noted that, in equation (26), the term $\frac{V_{shift}}{R_K}$ is the current flowing both in R_K and R_B in the transistor non-conducting state (assuming that $I_{co} \ll \frac{V_{shift}}{R_K}$). It is interesting that minimizing the power dissipated in R_K in the "transistor conducting" state resulted in an establishing of the necessary "shift" current in the non-conducting state.

The power dissipated in R_B in the conducting state is given by:

$$P_B = \left[\frac{V_{shift}}{R_K} + \frac{\Delta V_{be}}{R_B} \right]^2 R_B \qquad (28)$$

Introducing equation (26) as a constraint:

$$P_B = \left[I_B + \frac{2\,\Delta V_{be}}{R_B} \right]^2 R_B \tag{29}$$

Taking the first derivative with respect to R_B and setting it equal to zero, establishes the value of R_B which minimizes the power dissipated in R_B under the constraint that power is also minimized in R_K:

$$\frac{dP_B}{dR_B} = \left[I_B + \frac{2\,\Delta V_{be}}{R_B} \right]^2 - \frac{4\,\Delta V_{be}}{R_B} \left[I_B + \frac{2\,\Delta V_{be}}{R_B} \right] = 0 \tag{30}$$

$$\therefore \quad R_B = \frac{2\,\Delta V_{be}}{I_B} \tag{31}$$

In order to establish the variation of P_K and P_B with non-optimum values of R_B and R_K, substitute the following into equations (24) and (28):

$$R_B = k \left[\frac{2\,\Delta V_{eb}}{I_B} \right] \tag{32}$$

$$R_K = K \left[\frac{V_{shift}}{I_B + \frac{\Delta V_{eb}}{R_B}} \right] = K \left[\frac{V_{shift}}{\left(1 + \frac{1}{2k}\right) I_B} \right] \tag{33}$$

the result is that:

$$P_K = I_B \left[1 + \frac{1}{2k} \right] V_{shift} \left[K + 2 + \frac{1}{K} \right] \tag{34}$$

and

$$P_B = 2 I_B\, \Delta V_{eb} \left[k + 2 + \frac{1}{k} \right] \tag{35}$$

at K=1 and k=1, both P_K and P_B are at a minimum and given by:

$$\underline{P_K} = 6\, I_B\, V_{shift} \tag{36}$$

$$\underline{P_B} = 8\, I_B\, \Delta V_{eb} \tag{37}$$

The function $1/4\ (K + 2 + \frac{1}{K})$ is plotted in Figure 25. As might be expected, it has a minimum value at K equal one, and increases rapidly for decreasing K and moderately for increasing K. The function of K is the same as the function of k for P_B. Thus, Figure 25 shows the relative increase in either P_K or P_B as a function of any non-optimum ($K \neq 1$) choice of R_K or R_B.

The supply voltage E_B must be designed to correspond to the non-conducting state:

$$E_B = \left[I_B + \frac{\Delta V_{be}}{R_B} \right] R_B \tag{38}$$

substituting equation 32 for R_B:

$$E_B = (2k + 1)\ \Delta V_{be} \tag{39}$$

or under minimum power design

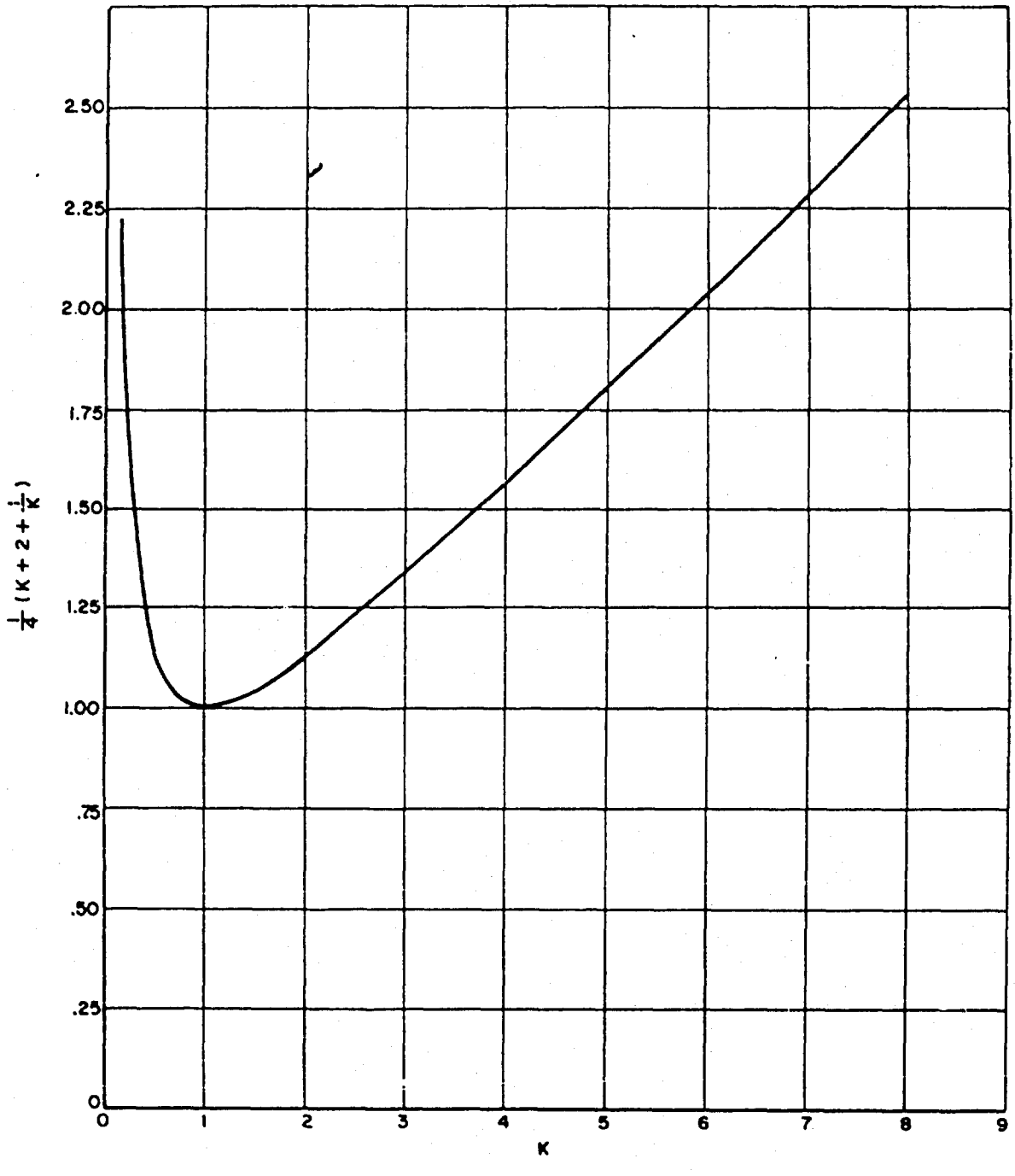
$$E_B = 3\ \Delta V_{be} \tag{40}$$

By applying the above equations, it is seen that the input load to R_K in the conducting state under minimum power design is characterized by a current which is three times I_B and a voltage which is equal to $\left[2\ V_{shift} + V_{be} \right]$. This load can be used to establish E_D and R_D by applying the Bi-State Nominal Design. Thus, it is found that for minimum power dissipation

$$E_D = 2 \left[2\ V_{shift} + V_{eb} \right] \tag{41}$$

$$R_D = \frac{E_D}{2(3\ I_B)} = \frac{2V_{shift} + V_{eb}}{3\ I_B} \tag{42}$$

In the DTL - NOR case, there is a base current - common emitter current gain design relationship similar to the DCTL - NOR case.



Variation of Power for Non-optimum Choice

Figure 25

In the case of the DTL-NOR, waste current and leakage current are not as important considerations. An approximate inequality which must be fulfilled is:

$$\underline{\beta} I_B \geq I_c \geq n_o \left[4 I_B + \frac{2Q}{t} \right] + n_i \left[I_R + \frac{Q_c}{t} \right]$$

$$\therefore \quad \frac{I_c}{\underline{\beta}} \leq I_B$$

$$\therefore \quad I_c \geq n_o \left[4 \frac{I_c}{\underline{\beta}} + \frac{2Q}{t} \right] + n_i \left[I_R + \frac{Q_c}{t} \right]$$

$$\therefore \quad \underline{\beta} \geq \frac{4 I_c \quad n_o}{I_c - 2 \left[n_o \frac{Q}{t} + \frac{n_i}{2} \left(I_R + \frac{Q_c}{t} \right) \right]}$$

where:

n_o = fan-out
n_i = fan-in
I_R = the reverse diode conduction current
Q_c = the average wiring capacitance
t = the switching time
$\underline{\beta}$ = the minimum acceptable common emitter current gain

b. DTL "NOR" Circuit Analysis

The problem of circuit design is generally one of matching a set of terminal requirements, based upon system considerations, to device and component characteristics in such a way that an "optimum" circuit is derived. When microelectronic circuits are involved, the optimum may be defined as the lowest power-dissipating circuit which is still able to meet all terminal requirements, or as the circuit having the highest tolerance to component drift while still meeting all terminal requirements. This report is concerned basically with establishing design criteria which may be useful in both the design and evaluation of a resistor - transistor - diode "Nand" or "Nor" gate.

Figure 24 illustrates a basic negative logic NOR configuration. (Using a pnp transistor with reversed battery polarities and diodes would yield a negative logic NAND circuit.) Since the transistor is used basically as a switch, there exist two quiescent states which a circuit designer must be concerned with. The first state will be referred to as the "conducting" state and implies that the transistor is in its saturated condition. The second state is referred to as the "non-conducting" state and refers to the cutoff condition of the transistor. When the circuit is in the conducting state, certain design criteria must be met which may be considerably different from those criteria applying when the circuit is in its non-conducting state. The static design problem consists of imposing constraining conditions upon the circuit in both of its states such that the terminal requirements of the circuit are met while making sure that the conditions of one state do not mutually exclude the conditions of the second state.

Hence, the static design procedure may be treated in a three-dimensional space as illustrated in Figure 26. The conducting state of the circuit can be represented as a design area on the z - x plane where the area is determined by the constraint conditions applied to the circuit during transistor saturation. Similarly, a design area can be specified for the non-conducting

state in the z - y plane. If the two areas are then projected in the y and z directions respectively, an intersection will occur which defines a design volume. Any circuit having the parameters x_i, y_i, z_i which fall within the intersected volume will meet the terminal specifications of the circuit for both circuit states. A large number of designs, having co-ordinates within the volume, would satisfy the terminal requirements. However, only one design would meet an optimum requirement, such as minimum power or maximum reliability. If the two areas do not intersect, then the terminal requirements imposed upon the circuit in its conducting state are not compatible with those of the circuit in its non-conducting state and, consequently, the terminal conditions would not be physically realizable.

It is apparent that this method of circuit design leads to a fairly convenient check on whether or not a given circuit meets terminal requirements. Once a circuit has been built according to a particular design, the circuit can be measured for those properties referred to as x, y, z in Figure 26. If the space co-ordinate falls within the intersected design volume, the circuit meets its terminal requirements: if not, the circuit should be rejected. It is apparent that the greater the intersected volume, the greater will be the probability that a fabricated circuit has x, y, z parameters satisfactory for meeting the circuit specifications. Thus, a small intersected design volume would indicate very tight circuit requirements which may be incompatible with some microelectronic fabrication techniques while a larger intersected volume would imply higher circuit yield in the manufacturing process.

The problem of setting up a design procedure as outlined above is essentially one of finding a parameter z which is common to both the non-conducting and conducting states of the circuit while finding suitable x and y parameters as well as constraining conditions to map out a design area on the x - z and y - z planes. Section 2 suggests such a procedure for the NOR gate illustrated in Figure 24.

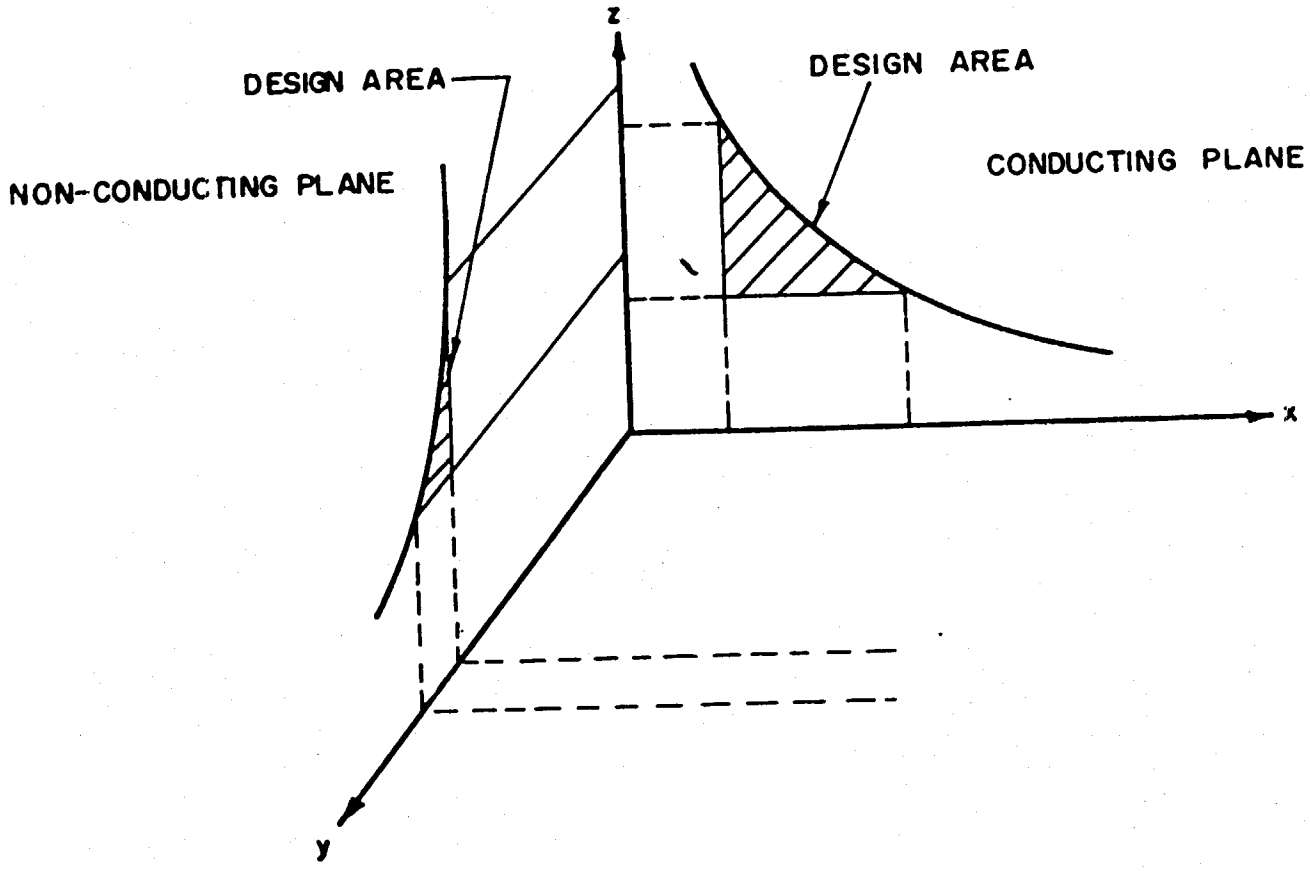


Figure 26. Design Problem from Geometric Point-of-view

Static Design Procedure

The static design procedure for the Nand gate of Figure 24 is concerned with finding suitable values for the four resistors, R_D, R_K, R_B and R_L. It will be assumed that the system designer imposes a fan-in requirement, n_i, a fan-out requirement, n_o, and available power supply potentials, E_D, E_B and E_{CC}. In addition, the system requirements may impose restrictions upon frequency, signal propagation delay, rise and fall times, etc. which affect the design of the circuit in a third state, viz., the transition state and its relationship to the static design will be considered in a later report.

For purposes of this analysis, assume that the transistor is specified in terms of its minimum low frequency current amplification factor, α_{EO}, its base to emitter saturation drop, V_{BES}, its collector to emitter saturation voltage, V_{CES}, and its leakage current, I_{CBO}. In addition, it will be assumed that the input diodes are specified in terms of their forward voltage drops, V_D, and reverse leakage. Thus, the model of the saturated transistor and the conducting diodes will be considered as simple batteries representing the various voltage drops during conduction. This model is justified in view of the fact that the circuit configuration using resistor interstage networks is based upon current control by the resistors and not by the active devices. If this criterion is not met, then the DTL configuration is not used to proper advantage.

Conduction State Parameters

When the transistor is saturated, it supplies current to an external load while being held in saturation by the current supplied from E_D. It is important to make sure that the drive current is of sufficient magnitude that the transistor stays clamped in its saturation state for the worst load conditions. Hence, an obvious parameter which the circuit designer must control is the digital current amplification of the saturated transistor,

defined as

$$A_i = I_c / I_B \tag{1}$$

It is essential that A_i never exceed the minimum low frequency amplification factor of the transistor in the conduction state of the circuit. If the current flowing through each logic diode is denoted by I_S, then the maximum load which the transistor will have to supply to its fan-out branches is

$$I_o = n_i \, n_o \, I_S \tag{2}$$

It is interesting to note from Equation 2 that high fan-in and high fan-out requirements impose potentially severe loading conditions on the transistors.

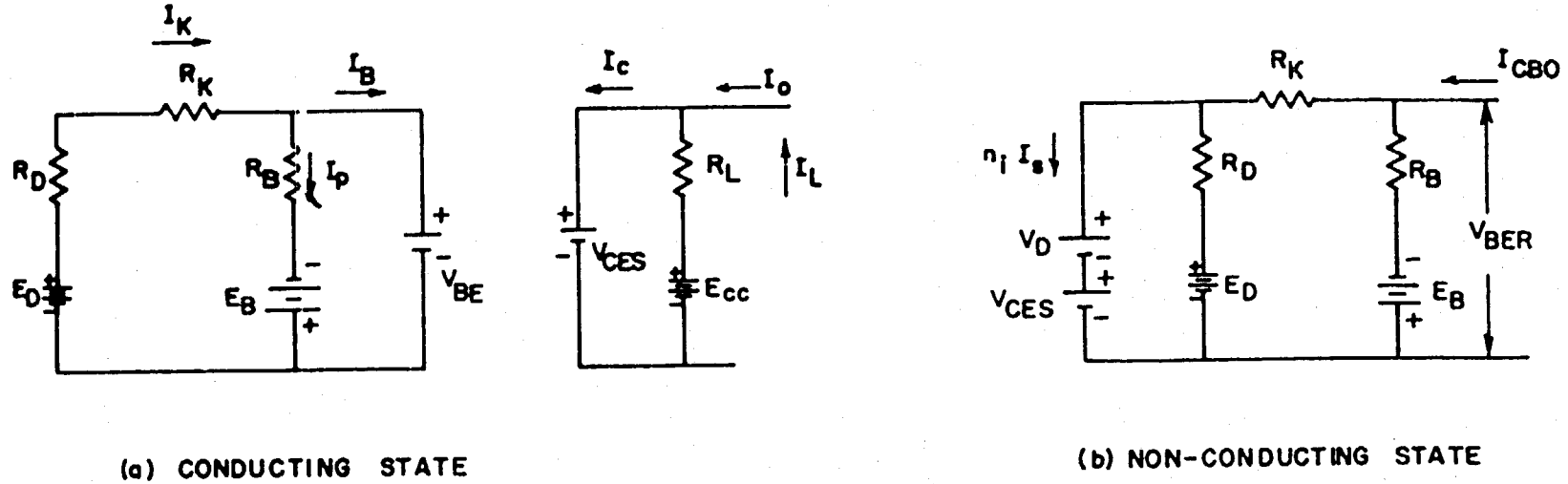
The next step in the analytical procedure is to derive the digital current amplification in terms of the circuit parameters for the equivalent circuit shown in Figure 27a. Thus:

$$A_i = \left[\frac{(n_i \, n_o \, I_S)(R_D + R_K)}{E_D - V_{BES}} \right] \left[\frac{1 + \dfrac{E_{CC} - V_{CES}}{n_i \, n_o \, I_S \, R_L}}{1 - \left(\dfrac{E_B + V_{BES}}{E_D - V_{BES}} \right) \left(\dfrac{R_D + R_K}{R_B} \right)} \right] \tag{3}$$

Since A_i is an important design variable, it is desirable to investigate Equation 3 more closely in order to determine whether or not other design parameters are inherent in the expression. It can be seen that Equation 3 may be written as follows:

$$A_i = \left(\frac{\gamma}{1 - \Psi} \right) \left(1 + \sigma \right) \tag{4}$$

where



(a) CONDUCTING STATE

(b) NON-CONDUCTING STATE

Figure 27. Approximate Equivalent Circuits for Static Design

$$\gamma = \frac{I_o}{I_K} = \frac{n_i \, n_o' \, I_S \, (R_D + R_K)}{E_D - V_{BES}} \tag{5a}$$

$$\sigma = \frac{I_L}{I_o} = \frac{E_{CC} - V_{CES}}{n_i \, n_o \, I_S \, R_L} \tag{5b}$$

$$\psi = \frac{I_P}{I_K} = \left[\frac{E_B + V_{BES}}{E_D - V_{BES}} \right] \left[\frac{R_D + R_K}{R_B} \right] \tag{5c}$$

The current ratio defined as γ may be considered as a current efficiency measure since it represents the amount of drive current required from the source E_D in order to supply the output load current, I_o. Since γ involves resistors R_D and R_K which are important in determining I_S during the non-conducting state of the circuit, it may be expected that γ will figure prominently as a design parameter for the non-conducting state of the circuit as well as for the conducting state. The current ratio, σ, is a fraction of the logic current which must be supplied to the nominal load resistor R_L. The current I_L performs no useful work as far as the static circuit requirements are concerned but is important in speed considerations as well as possible saturation control of the circuit. The current ratio ψ is particularly important since it figures prominently in the stability of the circuit during transistor conduction. For example, differentiating Equation 4 leads to the following digital current amplification variation:

$$\frac{dA_i}{A_i} = \left(\frac{d\gamma}{\gamma} \right) + \left(\frac{\sigma}{1+\sigma} \right) \left(\frac{d\sigma}{\sigma} \right) + \left(\frac{\psi}{1-\psi} \right) \left(\frac{d\psi}{\psi} \right) \tag{6}$$

The variational terms involving γ, σ and ψ in Equation 6 can be written as worst-case variations involving tolerances on the resistors and battery supplies. If this is done, it can be shown that the worst-case digital

current amplification variation is:

$$\frac{dA_i}{A_i} = (\delta_R + \delta_E) \left(\frac{1 + \psi}{1 - \psi}\right) \tag{7}$$

In Equation 7, δ_R is the percent variation in resistor values while δ_E is the percent variation of the power supplies. Hence, it is apparent that under worst-case deviations, the digital current amplification factor is most sensitive to the current ratio given by ψ in Equation 5c. For example, if ψ were equal to one-third, the worst-case variations in resistors and power supplies will be multiplied by a factor of two when reflected in the variation of the digital current amplification.

In view of the foregoing discussion, it seems desirable to establish a conducting state equation relating A_i to γ with σ and ψ as constraint parameters. The resulting conducting state plane is illustrated in Figure 28. A_i and γ are linearly related if σ and ψ are considered design parameters. The minimum value of both σ and ψ is equal to zero and consequently a straight line of 45° slope between A_i and γ represents one boundary of the design region. A maximum value of ψ may be specified by the circuit designer based upon bias stability considerations as given by Equation 7. A maximum value of σ may also be assigned based primarily upon speed considerations. Thus, a second straight line relating A_i to γ may be obtained representing an upper boundary for the design region. A constraining condition on the digital current amplification, which insures transistor saturation under maximum load, is that A_i must be less than the minimum value of the low frequency current amplification factor of the transistor. This condition imposes a third boundary on the design region. It can also be shown that for design realizability, the value of γ must exceed the fan-out factor n_o multiplied by $(1 - \psi)$. This realizability constraint imposes a fourth boundary on the design region and encloses the area given by ABCD in Figure 28. However, further constraints are usually necessary. For

example, noise considerations may dictate a minimum saturation margin which would further reduce the allowable digital current amplification. Applying the saturation margin constraint to the design plane results in a reduction in the design region shown in Figure 28 from the original area to a new area denoted by A'BC'D. In addition, it is desirable to impose tolerance constraints on the circuit design. It is necessary, for example, that the saturation margin condition be met despite variations in resistor and battery values. Applying Equation 7 to the conduction plane of Figure 28 results in further narrowing of the design region to the new area given by A"BC"D. If these are all the constraints that are applied to the conduction state of the circuit, the final design region for the conduction state will be given by the area A"BC"D. If the circuit designer selects specific values for σ and ψ the design region will be reduced from an area to a line within the design region. In any event, an infinite number of designs will theoretically satisfy the conduction state requirements.

The remaining problem in the design of the NOR gate is to derive a similar design region for the non-conducting state of the circuit which may be referenced to the design region of the conducting state.

Non-Conduction State Parameters

When the transistor is in the cutoff condition, current I_D flows through the logic load of the preceeding gate. Consequently, the non-conducting state of the circuit determines the value of I_S. The value of I_S will generally be selected on the basis of the diode properties as well as from speed considerations. Thus, I_S is one of the design parameters which should be initially selected and it is important to derive the value of I_S in terms of the equivalent circuit illustrated in Figure 27b. Hence,

$$I_S = \left(\frac{E_D - V_D - V_{CES}}{n_i R_D}\right)\left[1 - \left(\frac{E_B + V_D + V_{CES}}{E_D - V_D - V_{CES}}\right)\left(\frac{R_D}{R_K + R_B}\right)\right] \qquad (8)$$

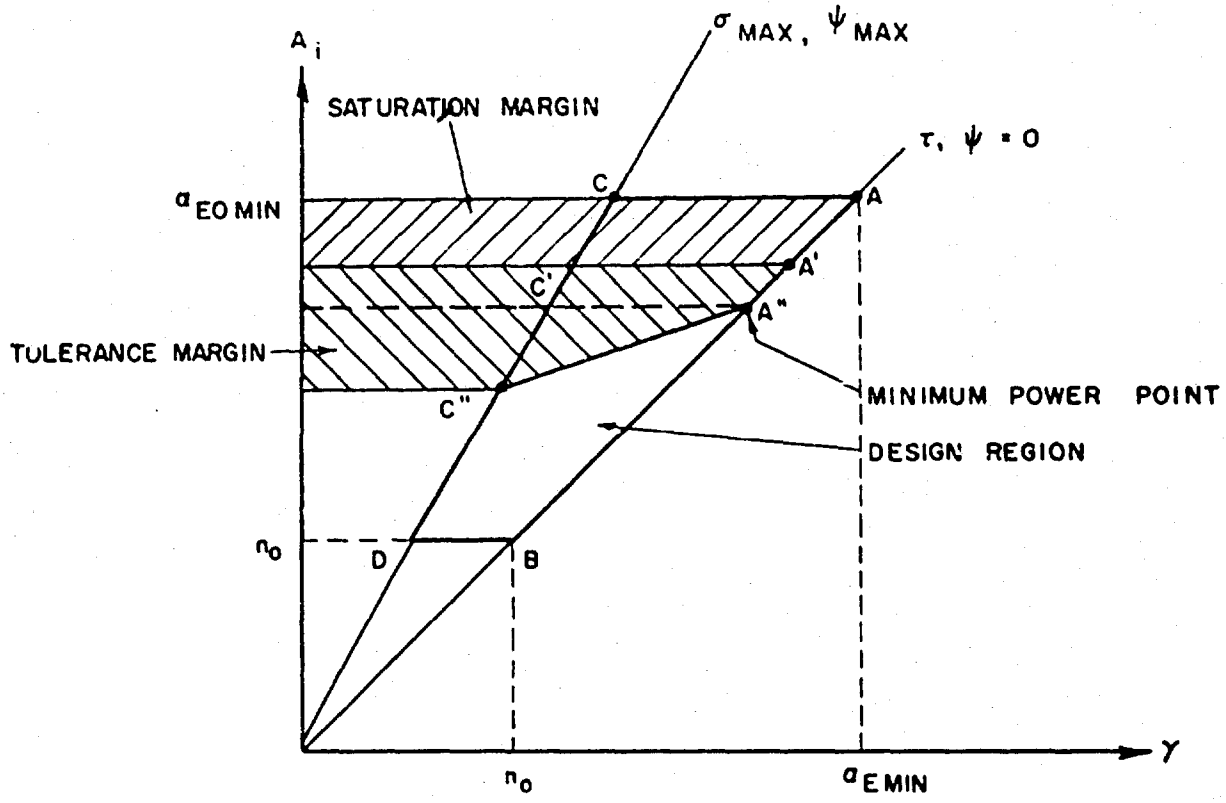


Figure 28. Design Region for Conducting State

Another important design parameter in the non-conducting state of the circuit is the value of the base to emitter voltage of the transistor. The base to emitter voltage in the non-conducting state will be denoted by V_{BER}. The bias battery E_B insures that the transistor will remain cutoff despite the leakage current, I_{CBO}, and provides a threshold margin which may be used to insure transistor cutoff despite circuit noise. It is important, therefore, to calculate the value of V_{BER} in terms of the equivalent circuit in Figure 27b.

$$V_{BER} = \frac{V_D + V_{CES} + I_{CBO} R_K - \frac{R_K}{R_B} E_B}{1 + \frac{R_K}{R_B}} \qquad (9)$$

Equations 8 and 9 fully describe the d-c conditions of the NOR gate in its non-conducting state. The design problem is now to relate Equations 8 and 9 to Equation 4 such that one of the design parameters of Equation 4 is explicit in both Equations 8 and 9. In order to confine the problem to a three-dimensional space, it would also be desirable to combine Equations 8 and 9 so that only one additional design parameter is added to A_i and γ. A fairly unwieldy expression can be avoided if the following inequality is satisfied:

$$\left(\frac{E_B + V_D + V_{CES}}{E_D - V_D - V_{CES}}\right) \left(\frac{R_D}{R_K + R_B}\right) << 1 \qquad (10)$$

It should be recognized that the left-hand side of inequality 10 is the ratio of the current supplied by E_B to the current supplied by E_D comprising the signal current $n_i I_S$ (see Figure 27b. If the resistors R_K and R_B properly isolate the input diodes from the base bias supply of the transistor, then inequality 10 generally should be satisfied. Hence, I_S may be approximated by:

$$I_S = \frac{E_D - V_D - V_{CES}}{n_i R_D} \tag{11}$$

Substituting Equation 11 into Equations 5a and 5c and solving for the ratio of R_K to R_B and the resistance value R_K results in

$$\frac{R_K}{R_B} = \Psi \left(\frac{E_D - V_{BES}}{E_B + V_{BES}} \right) \left[\frac{n_i I_S R_K}{n_i I_S R_K + (E_D - V_D - V_{CES})} \right] \tag{12}$$

$$R_K = \left(\frac{E_D - V_{BES}}{n_i n_o I_S} \right) \left[\gamma - n_o \left(\frac{E_D - V_D - V_{CES}}{E_D - V_{BES}} \right) \right] \tag{13}$$

Equations 12 and 13 may now be substituted into Equation 9 in order to obtain an expression of V_{BER} involving design parameters that were used to determine the conducting state of the circuit. It is convenient to define several ratios of currents and voltages prior to writing the new equation for V_{BER}. Thus,

$$B_L = \left(\frac{I_{CBO\ MAX}}{n_i n_o I_S} \right) \left(\frac{E_D - V_{BES}}{V_D + V_{CES}} \right) \tag{14a}$$

$$B_1 = \frac{E_D - V_D - V_{CES}}{E_D - V_{BES}} \tag{14b}$$

$$B_2 = \frac{E_D - V_{BES}}{E_B + V_{BES}} \tag{14c}$$

$$B_3 = E_B / (V_C + V_{CES}) \tag{14d}$$

The base to emitter voltage can then be written as follows:

$$\frac{V_{BER}}{V_D + V_{CES}} \triangleq T_V = \frac{1 + (\gamma - n_o B_1)\left(B_L - \frac{\Psi}{\gamma} B_2 B_3\right)}{1 + (\gamma - n_o B_1)\left(\frac{\Psi}{\gamma} B_2\right)} \qquad (15)$$

If the ratio V_{BER} to $(V_D + V_{CES})$, defined as T_V in Equation 15, is selected as a dependent variable of the non-conducting state design equation and γ is selected as the independent variable, a relationship is established which allows constraint conditions to be mapped out in the non-conducting plane which can then be related to the conducting plane in a three-dimensional space given by the co-ordinates γ, A_1 and T_V. Establishing the constraint conditions for the non-conducting state, or the T_V - γ plane, is the next problem.

In order to determine the design region in the non-conducting plane, it is best to start by considering the absolute maximum allowable base to emitter voltage for the cutoff transistor. This potential is generally referred to as the threshold voltage, viz., the voltage below which the transistor is considered cut off and above which the transistor is considered in a state of semi- or full-conduction. Denoting the threshold voltage by V_{BEC}, the ratio of V_{BEC} to $(V_D + V_{CES})$ establishes the upper bound of T_V. In general, however, it is not tolerable to allow the base-to-emitter bias voltage to reach the threshold point. Consequently, a threshold margin is specified which in fact provides the maximum allowable value of T_V. This upper bound is illustrated by the line F' - F' in Figure 29.

The lower bound for T_V as a function of γ may be calculated from Equation 15 by using the maximum value of Ψ as determined for stability considerations relating to Equation 7.

A minimum value of γ can be established from Equation 13 by noting that R_K must always be positive. In addition, it is apparent from Equation 4 that γ must always be less than the minimum current amplification factor of

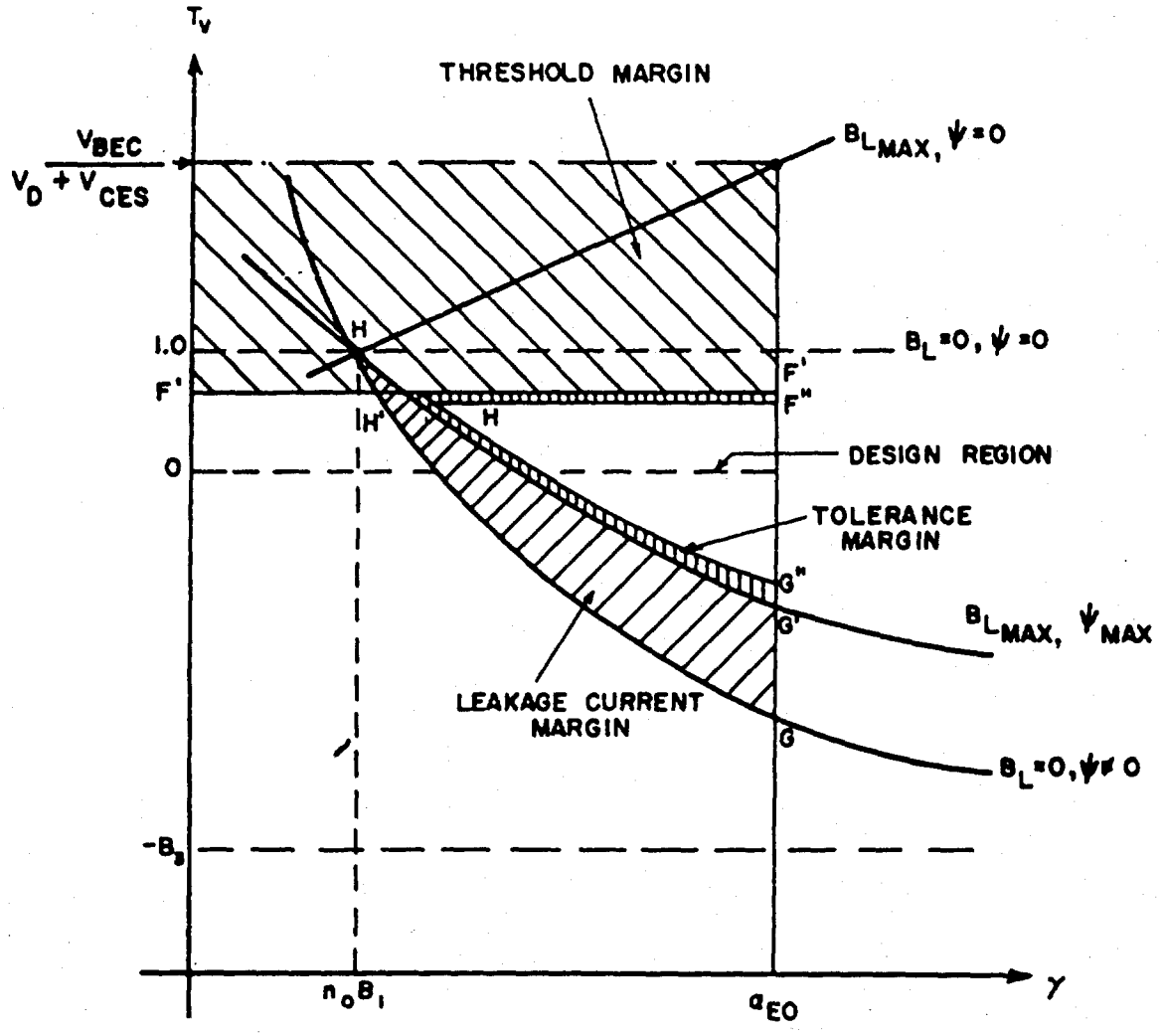


Figure 29. Design Region for Non-conducting State

the transistor, α_{EC}. Consequently, upper and lower bounds may readily be established for γ in the T_V - γ design plane. Thus, an area is enclosed mapping out the permissible design region for the non-conducting state of the Nand circuit.

This design region may be further constrained by applying resistor and voltage supply tolerance considerations to Equation 15. Study of the tolerance problem shows that the worst case deviations of resistors and battery supplies assumed for the conducting state of the circuit happens to be a favorable type of deviation for the non-conducting state insofar as the deviations increase the threshold margin. However, if a designer wants to be ultra conservative, it is readily shown that the lower bound of T_V may be further constrained by assuming a worst case deviation in resistors and batteries leading to a percent variation in T_V given by

$$\frac{d\,T_V}{T_V} = \left[\frac{1}{1 + (R_K/R_B)}\right] (2\,\delta_R + \delta_E) \qquad (16)$$

This tolerance condition further narrows the design region in the non-conducting plane as illustrated in Figure 29. The final design region shown in Figure 29 encompasses those circuit designs which meet the requirements of the Nand gate in its non-conducting state.

Complete Static Design

The static design for the NOR circuit of Figure 24 can now be undertaken simultaneously for the conducting and non-conducting states of the circuit. The procedure is as follows. First, the design region for the conducting state of the circuit is mapped as illustrated in Figure 28. Second, using γ as the common independent variable, the design region is mapped for the non-conducting state of the circuit, as illustrated in Figure 29. Finally, theintersection of the two design regions is determined by finding the range of γ values which lie in both design regions.

This procedure is illustrated in Figure 30. The shaded areas of the two design regions encompass those values of A_i, γ and T_V which are mutually compatible with the circuit specifications and various design constraints. The specific design may be narrowed to a single point in the A_i, γ, T_V space by imposing one or more optimizing criteria. For example, referring to Figure 30 the design which satisfies the terminal requirements of the circuit and is also a minimum power design lies at the point A"X.

Once allowable design regions have been established for the conducting and non-conducting states of the circuit, a fabricated circuit can readily be tested to determine whether or not it meets terminal requirements by measuring its A_i, γ and T_V in order to determine whether or not it falls within the shaded regions of the design space shown in Figure 30. Since two of the co-ordinates are current ratios while one co-ordinate is a voltage ratio, six terminal measurements are required to determine circuit acceptability. Thus, the design procedure described above may be used in reverse to check circuits against terminal specifications.

Analytic Procedure

It may sometimes be desirable to use an analytic procedure directly for the design of the NOR gate rather than the graphical procedure illustrated in Figure 30. A procedure for such an analytical design is outlined in Table I, where some of the graphical steps have been reduced directly to analytic form. An example of a circuit design according to the procedure outlined in Table I is given in Table II.

Power Considerations

It is of interest to analyze the power requirements of the NOR gate shown in Figure 30 in order to determine what circuit parameters and design variables contribute most to power dissipation. For the conducting state of the circuit, the power dissipation is given by

$$P_C = E_D I_K + E_B I_P + E_{CC} I_L + I_O V_{CES} \qquad (17)$$

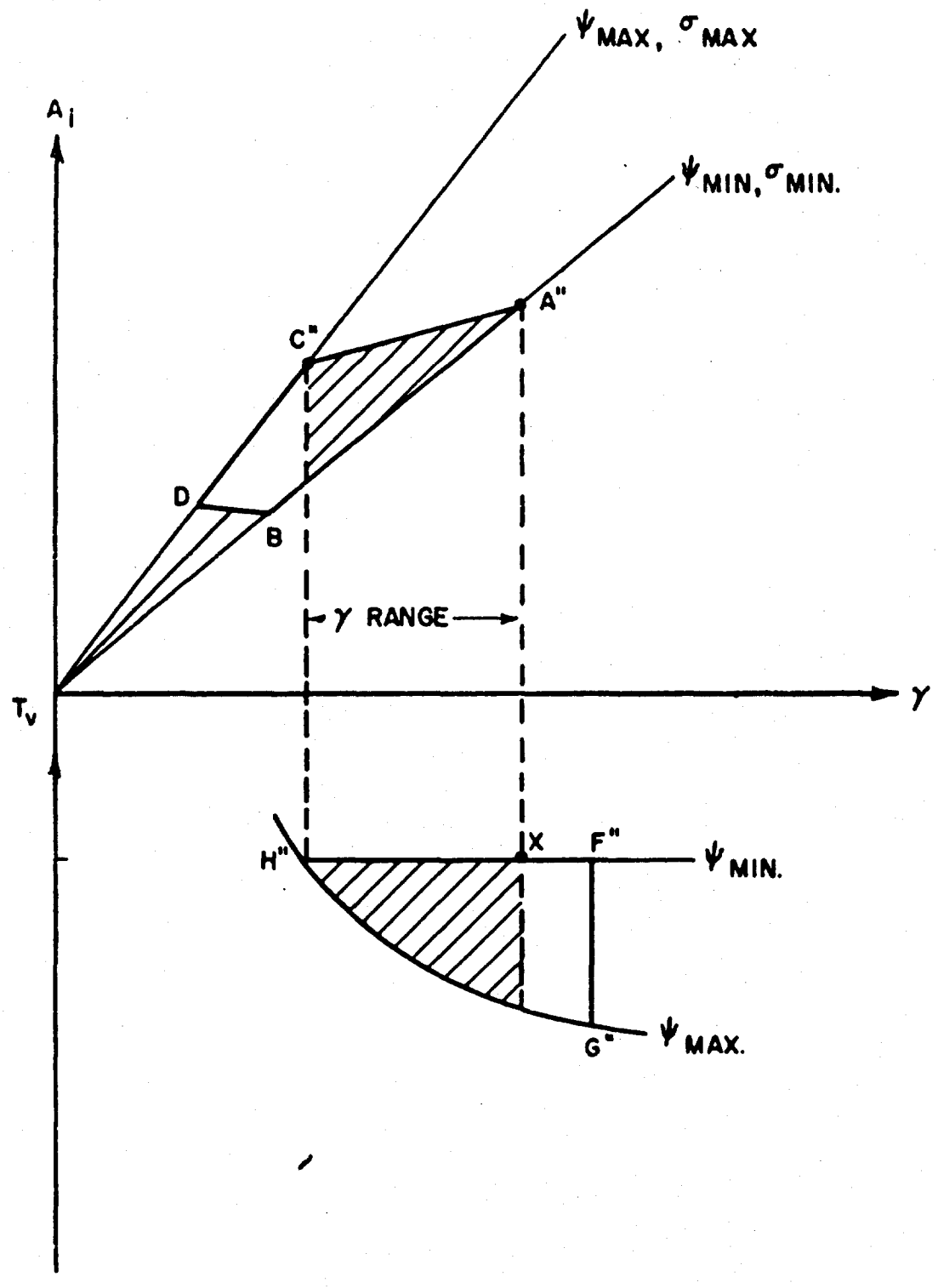


Figure 30. Compatible Design Region for Two States of Circuit

TABLE I

Synthesis Procedure - NOR Gate

1.) Given:

(a) System Specifications: E_D, E_B, E_{CC}, n_i, n_o, ∂_E

(b) Device Properties: $\alpha_{EO\ MIN}$, $I_{CBO\ MAX}$, V_{BES}, V_{CES}, V_D, ∂_R

2.) Select: I_S, Ψ , σ

3.) Calculate:

(a) $B_1 = \dfrac{E_D - V_D - V_{CES}}{E_D - V_{BES}}$

(b) $B_2 = \dfrac{E_D - V_{BES}}{E_B + V_{BES}}$

(c) $B_3 = \dfrac{E_B}{V_D + V_{CES}}$

(d) $B_L = \left(\dfrac{I_{CBO\ MAX}}{n_i\ n_o\ I_S} \right) \left(\dfrac{E_D - V_{BES}}{V_D + V_{CES}} \right)$

4.) Derive γ as function of T_V:

(a) If $B_L << \Psi / B_2\ B_3\ n_o$

$$\gamma = \frac{n_o\ \Psi\ B_1\ B_2\ (B_3 + T_V)}{1 - \Psi\ B_2\ B_3 - T_V\ (1 + B_2\ \Psi)}$$

(b) If B_L is not negligible, solve:

$$\gamma^2 + \gamma \left(\frac{1}{B_L} \right) \left[1 - \Psi\ B_2\ B_3 - n_o\ B_1\ B_L - T_V\ (1 + \Psi\ B_2) \right] +$$

$$n_o\ \Psi \left(\frac{B_1\ B_2}{B_L} \right) (B_3 + T_V) = 0$$

TABLE I (Continued)
Synthesis Procedure - NOR Gate

5.) Select T_V so that:

$$\frac{\alpha_{EO\ MIN}}{\left(\frac{1+\sigma}{1-\psi}\right)\left[1+(\partial_R+\partial_E)\left(\frac{1+\psi}{1-\psi}\right)\right]} > \gamma > n_o$$

6.) Calculate γ from (4) and (5).

7.) Calculate resistor values:

(a) $R_D = \dfrac{E_D - V_D - V_{CES}}{n_i\ I_S}$

(b) $R_K = \dfrac{E_D - V_{BES}}{n_i\ n_o\ I_S} \qquad (\gamma - n_o\ B_1)$

(c) $R_B = \dfrac{1}{\psi\ B_2} \qquad (R_D + R_K)$

(d) $R_L = \dfrac{E_{CC} - V_{CES}}{\sigma\ n_i\ n_o\ I_S}$

TABLE II

Design Example

1.) Given: $E_{CC} = E_D = 3$ v., $E_B = 3$ v., $n_i = 5$, $n_o = 4$, $\partial_E = \pm 10\%$

$\alpha_{EO\ MIN} = 20$, $I_{CBO\ MAX} = 0.1\ \mu a$, $V_{BES} = V_D = 0.7$ v.,

$V_{CES} = 0.3$ v., $\partial_R = \pm 10\%$

2.) Select: $I_S = 0.5$ ma, $\Psi = 0.5$, $\sigma = 0.2$

3.) Calculate:

(a) $B_1 = \dfrac{3 - 0.7 - 0.3}{3 - 0.7} = 0.87$

(b) $B_2 = \dfrac{3 - 0.7}{3 + 0.7} = 0.62$

(c) $B_3 = \dfrac{3}{0.7 + 0.3} = 3$

(d) $B_L = \left(\dfrac{10^{-7}}{10^{-2}}\right)\left(\dfrac{3 - 0.7}{0.7 + 0.3}\right) = 2.3 \times 10^{-5}$

4.) Since $2.3 \times 10^{-5} << \dfrac{0.5}{(.62)\ (3)\ 4}$

(a) $\gamma = \dfrac{(4)\ (0.5)\ (0.87)\ (0.62)\ (3 + T_V)}{1 - (0.5\ (0.62)\ (3) - T_V \left[\ 1 + (0.62)\ (0.5)\ \right]}$

$$\gamma = \frac{(1.08)\ (3 + T_V)}{0.7 - 1.31\ T_V}$$

TABLE II (Continued)
Design Example

5.) However

$$\frac{20}{\left(\frac{1.2}{0.5}\right)\left[1 + (0.2)\ \frac{1.5}{0.5}\right]} > \gamma > 4$$

$$5.2 > \gamma > 4$$

6.) Select $T_V = -0.53$

So that $\gamma = 5.0$

7.) (a) $R_D = \frac{3 - 0.7 - 0.3}{(5)\ (.5)\ (10^{-3})} = 800\ \Omega$

(b) $R_K = \frac{(3 - 0.7)}{10^{-2}} \left[5 - (4)\ (.87)\right] = 350\ \Omega$

(c) $R_B = \left[\frac{1}{(0.5)\ (0.62)}\right] (1150) = 3700\ \Omega$

(d) $R_L = \frac{3 - 0.3}{(0.2)\ (10^{-2})} = 1350\ \Omega$

Equation 17 can be written in terms of the design variables and design parameters used in the analysis described above as follows:

$$P_C = (n_i\ n_o\ I_S\ E_{CC}) \left\{ \frac{V_{CES}}{E_{CC}} + \sigma + \left(\frac{E_B}{E_{CC}} \right) \left[\frac{\psi\ (1 + \sigma)}{A_i\ (1 - \psi)} \right] + \left(\frac{E_D}{E_{CC}} \right) \left[\frac{1 + \sigma}{A_i\ (1 - \psi)} \right] \right\} \tag{18}$$

It is apparent from Equation 18 that a minimum power design would require low values of σ and ψ and high values of the digital current amplification. For σ and ψ equal to zero, the circuit power dissipation in the conducting state would be

$$P_{C\ MIN} = (n_i\ n_o\ I_S\ E_{CC}) \left[\left(\frac{1}{A_i} \right) + \left(\frac{V_{CES}}{E_{CC}} \right) \right] \tag{19}$$

Analysis of the power dissipation of the circuit in its non-conducting state can similarly be made whereby it can be shown that the minimum power dissipation for the non-conducting state is

$$P_{N\ MIN} = n_i\ I_S\ E_D \tag{20}$$

Here again it has been assumed that σ and ψ are equal to zero. If the circuit is operated on a 50% duty cycle between conducting and non-conducting states, the average minimum power dissipation would be

$$\overline{P}_{MIN} = \left(\frac{I_S\ E_{CC}}{2} \right) \left[\frac{n_i\ n_o}{A_i} + \frac{n_i\ n_o\ V_{CES}}{E_{CC}} + n_i \right] \tag{21}$$

It can be seen from Equation 21 that the product of the fan-in and fan-out factors can greatly influence the power dissipation of the circuit unless transistors having low collector to emitter saturation voltages are used and unless digital current amplification of the transistors is kept high. The very minimum power dissipation possible for ideal transistors would be just equal to one-half of the fan-in factor times the diode load current I_S and the battery supply E_{BB}. Since I_S is usually selected on the basis of speed and noise considerations, it is apparent that with ideal devices, only speed and noise dictate the minimum power level of the circuit operation. However, as stabilization considerations are introduced in the circuit design, such as the variation of α_{EO} as a function of the temperature and operating point, transistor leakage current, component tolerances, etc., the minimum power dissipation may go up considerably. This should be particularly recognized by circuit designers who tend to over-design with worst case procedures.

B. OPTIMUM TOLERANCE SELECTION

This section describes work done in connection with techniques for the selection of optimum component tolerance in circuit design. It has been postulated that an optimum tolerance point exists for components of a circuit which yields a maximum value of reliability for either catastrophic or drift failures. The problem is to determine the optimum tolerance point for maximizing specific circuit designs. Conventional "worst case" design techniques and statistical design techniques are discussed briefly in order to provide background for the material which follows.

1. Definitions

For purpose of classification, some basic definitions are made. However, a general background in probability theory is assumed in the subsequent report.

1.1 Catastrophic Failure

Catastrophic failure is "open" or "short" of any circuit component. Further, assume that for a non-redundant circuit (or system) consisting of n components, the probability of catastrophic failure is given by:

$$P(c) = 1 - (1 - P_1)(1 - P_2) \ldots (1 - P_n)$$

$$= 1 - \prod_{i=1}^{n} (1 - P_i)$$

(where P_i $i = 1,2, \ldots, n$ are the respective catastrophic failure probabilities of the components). That is to say, the circuit (or system) fails if one or more component fails catastrophically. Notice the occurrence of such failures are usually random in nature. This leads to the assumption of constant failure rate with respect to time. This rate, however, is a function of both ambient temperature and electrical stress.

1.2 Drift Failure

Drift failure of a circuit is defined here as the failure to meet all circuit specifications (power gain, voltage/current level, stability, etc.) due

to variations in component (resistors, power supplies, transistor parameters) values from their nominal values. Usually, the circuit performance functions y_1, y_2, y_n are specified in terms of inequalities such as:

$$y_1 \geq A$$

$$B \geq y_2 \geq C \quad \text{etc.}$$

An illustration of the probability of drift failure, $P(y_1)$ versus the variable, y_1, is shown in Figure 31.

Hence, if one or more specification limits is exceeded due to component drift, the circuit has failed by definition. The probability of a particular specification exceeding its limit may be easily calculated once the probability density function of the performance function is known.

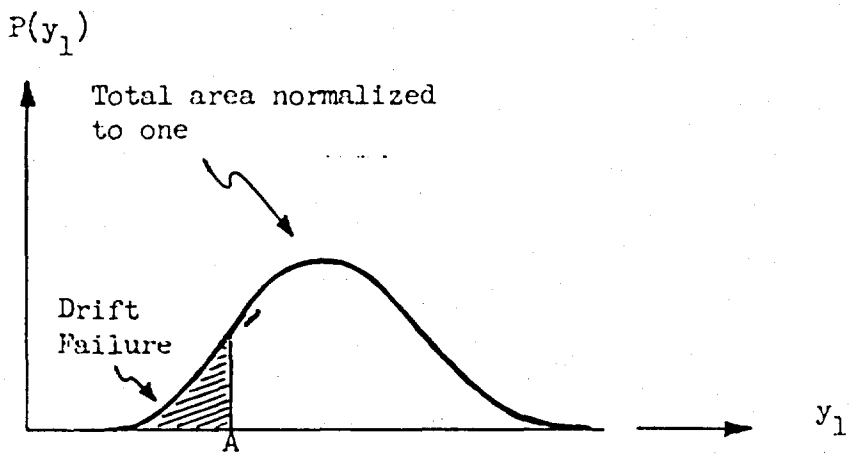


Figure 31. Probability of Drift Failure Curve (Specificiation $y_1 \geq A$)

The method for obtaining the probability density functions of circuit performance functions (or more directly, the calculation of drift failure) in terms of given component probability density functions will be discussed in a later section. However, it should be noted here that the probability of drift failure of a given circuit is given by one minus the probability that all the specifications are met.

1.3 Component Probability Density Functions

Any circuit component is subject to an initial manufacture tolerance, i.e., before any component is put into actual use, its initial value is described by an initial probability density function. This may vary from a gaussian form to some non-mathematically expressible curve. After the component with a predetermined initial value is put into actual use, the value of this component will again vary with time and under various operating environments. This variation may also be described by another probability density function, the shape of which depends both on the particular component in question and the particular environment it is subject to during the operating interval of the circuit. It is thus important to distinguish the two types of component density functions. The former may be made to approach an impulse function by tightening the manufacturer's tolerance, however, the latter is unavoidable. For the purpose of this study, the component probability density function is taken to include both the above independent effects.

1.4 Worst Case Design

Worst case design means that the circuit (or system) is designed in such a way that it should still operate (i.e., all specifications are satisfied) even under the "worst possible" combination of circuit component values. For purpose of illustration, the relay circuit in Figure 32 is used as an example.

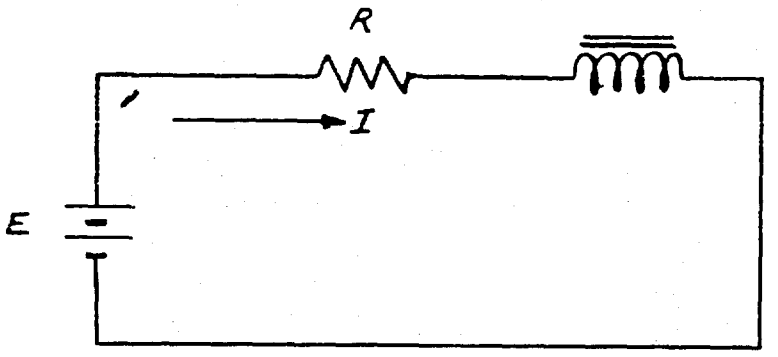


Figure 32. Relay Circuit

The only specification of the circuit is that the current I should exceed some threshold value I_o in order for the relay to operate. Hence, if

given a battery with nominal value E_o and maximum possible variation $\pm$ dE (%) from this value within the life time of the circuit, and also given $\pm$ dR (%) as the maximum possible variation of any resistor from its nominal value within the same life time, then the resistor should be chosen such that the following holds:

$$R \leq \left(\frac{E_o}{I_o}\right) \left(\frac{1 - dE}{1 + dR}\right)$$

Thus a "worst case" design essentially eliminates the possibility of circuit failure due to component drifts. Suppose, in the example above, the given power supply and any resistor are described by the following fictitious probability density functions:

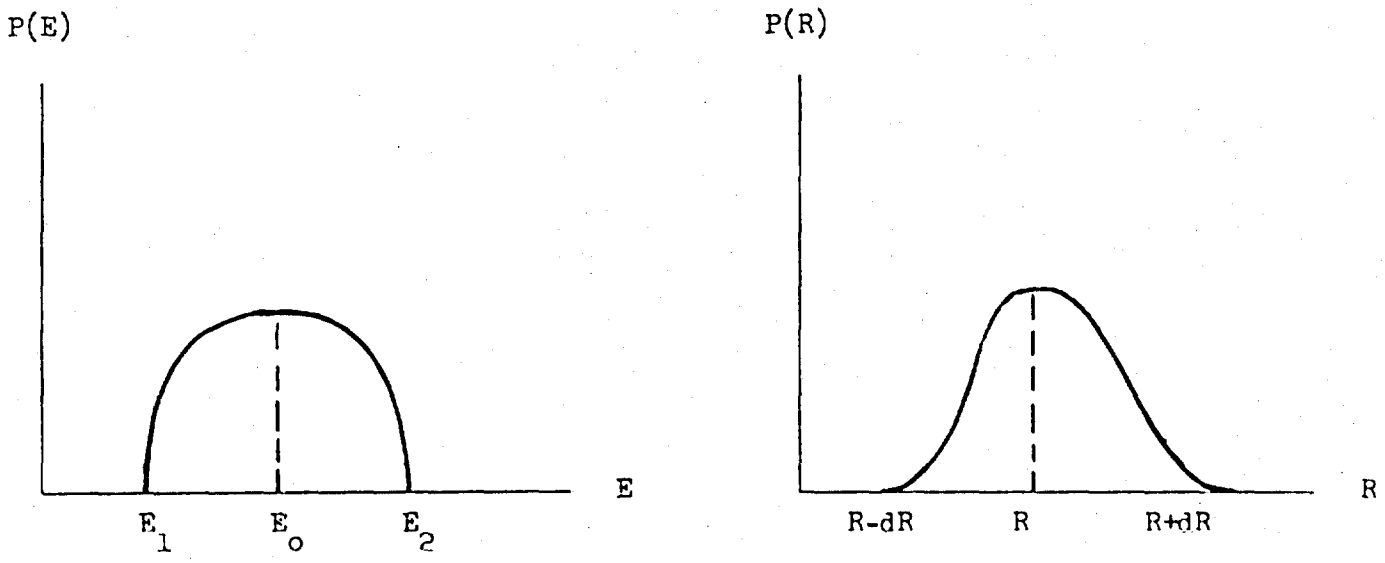


Figure 33. Probability Density Functions of R and E

Then it is obvious that a worst case design would require a choice of resistor value such that $R = \frac{E_1}{I_o(1+dR)}$. This choice eliminates the probability of having $I < I_o$, hence the probability of drift failure would be zero.

2. Statistical Design of Circuits

The objective of designing circuits statistically is to utilize the

knowledge of known probability density functions of circuit components to obtain a set of nominal component values which optimizes the circuit with respect to certain given criteria, such as the minimization of power dissipation for given reliability, the maximization of reliability for a given power level, or the minimization of the probability of catastrophic or drift failure. It should be noted that the optimum set of nominal component values does not necessarily guarantee worst case proof. One starts by picking randomly a set of nominal values for the various components needed in the circuit. The values may be picked anywhere from zero to infinity since no a-priori knowledge is assumed for the range of interest. Once the set of nominal values is chosen a statistical analysis is made on the basis of the required criteria using the knowledge of the given probability density functions of the components. Another set of nominal values is then picked. Notice this choice should be independent of the previous, i.e., one is just as random as the other and similarly an analysis is made to test the required criteria. This process of random picking and analyzing may go on many times to insure the result is within a certain confidence limit. The set of nominal values which meets the required criteria with the maximum probability is thus the optimum set. Hence, a true statistical design is, in a sense, a random process which yields an optimum set of nominal values as a final answer.

In the present study of optimum tolerance design the optimum set of nominal values should correspond to a particular set of component design tolerance. Hence, the random approach of statistical design is no longer applicable. In order to resolve the problem, a compromise between the "worst case" design method and the statistical design procedure is utilized. The detailed method employed in the present study is described in a later section.

Since the "random picking" of component values is no longer compatible with the present problem, the components must be chosen in a systematic manner with tolerance as a variable of design. In fact, the "worst case" equations are used in synthesizing the circuit with the selection of design tolerances less than the maximum possible component tolerance. That is to say, given the maximum possible drift, $\pm \Delta X$, which shall be referred to as fixed tolerance of the component X, the circuit should be synthesized with the worst case

equations but with design tolerance, dX, a variable of design less than ΔX.

2.1 Drift Failure

From the definition of drift failure it is clear that one may obtain the probability of drift failure from the probability density functions of the various circuit performance functions (y). If the equations of analysis are given together with the component density functions, the problems may be stated mathematically as follows; given a set of equations

$$y_i = f_i (X_1, X_2, \ldots, X_n) \qquad i = 1, 2 \ldots . m.$$

and the probability density functions of the X's, how does one obtain the probability density functions, $P(y_1)$, $P(y_2)$, ... $P(y_m)$? Or more directly, how does one obtain the probability that all the specifications are met?

2.2 The Monte Carlo Method

With the aid of a computer, the equations of the analysis may be solved many times by picking the component values according to the respective component density functions. (See Appendix B-3) The number of times that one or more performance functions fail to meet the specifications divided by the total number of trials corresponds to the probability of drift failure. Statistically, the accuracy of the result increases as the number of trials increases. This method has many advantages over the analytical methods. First, the applicability of the method is independent of the types of the component density functions. Secondly, the drift failure probability may be obtained directly without first solving for the probability density functions of the performance functions. Furthermore, the correlation between the various performance functions are taken into account automatically. Hence, for relatively complex circuits where more than one performance function is specified, the Monte Carlo method is useful in calculating the drift failure probabilities.

2.3 Catastrophic Failure

The probability of circuit catastrophic failure may be determined on the basis of currently available data on component catastrophic failure rates. These data are usually given as a function of both ambient temperature and

electrical stress level (power dissipation). Since the temperature requirement of a circuit is often specified, one needs only to calculate the power being dissipated in each component.

3. Numerical Results

The results presented here are obtained by utilizing the model presented in Appendix B-1 together with the material of Appendices B-2 and B-3. A second method for selecting optimum tolerances to maximize reliability for which numerical results have not been obtained is presented in the material of Appendix B-4. It is pointed out that the model of Appendix B-4 would be quite useful provided that types of data indicated were available.

3.1 Worst Case Circuit Design

The circuit shown in Figure 34 has been used in the analysis. The circuit component values for the static condition have been synthesized with worst case equations on a computer (see Appendix B-2) The specifications utilized in the synthesis are given in Table III.

The results of the static design synthesis are given in Table IV. In Table II are shown the nominal values of resistance corresponding to various values of tolerance. It is pointed out that the supply voltages, E_C and E_B, were allowed to deviate by the specified tolerance. For example, E_C and E_B were allowed to deviate $\pm$ 5% from their nominal values given in Table I in design of the circuit corresponding to $\pm$ 5% tolerance. Transistor parameter values were treated as constants in the design procedure.

Figure35 shows power dissipation versus per cent tolerance. Note that the power dissipation increases very rapidly, almost exponentially, with increasing tolerance.

3.2 Probability of Non Drift Failure

The probability of non drift failure, P(D), for the four circuits was computed by utilizing the procedures and the computer program described in Appendix B-3. The four circuits were tested with 11 distributions to $\pm$ 30%) with a sample size of 1600. These data are plotted in Figure 36.

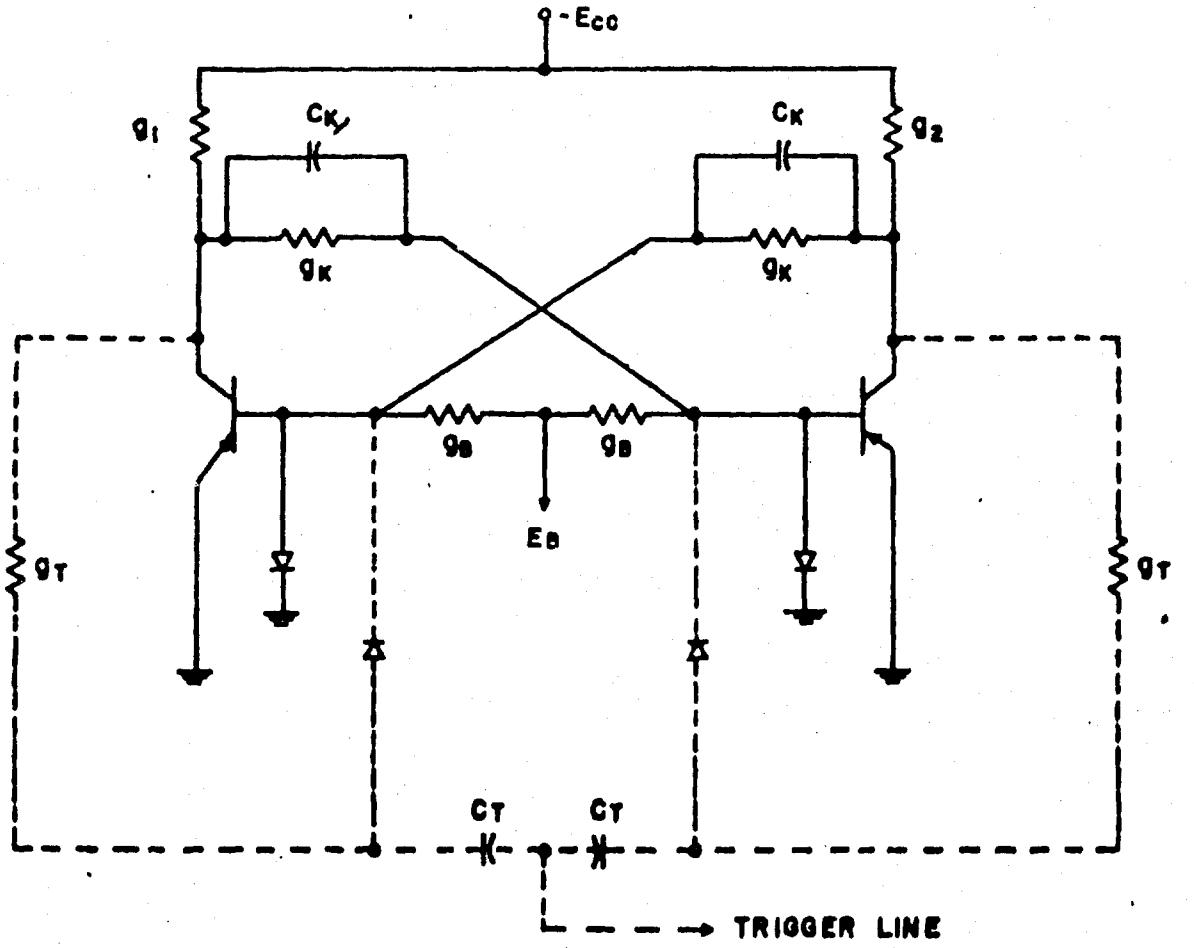


Figure 34. Saturating Base Returned Flip-flop Configuration (The dotted lines show a single point triggering system.)

TABLE III

DATA (CONSTANTS AND SPECIFICATIONS) FOR THE COMPUTER PROGRAM

1. I_c vs. β

2N335	
$I_{c(MA)}$	β
0.1	44
0.5	53
0.6	54
0.7	55
0.8	55
0.9	56
1.0	56
1.5	55
2.0	54
3.0	51
4.0	46

2. $E_c = 6$ Volts
3. $E_B = 2$ Volts
4. $V_1 = 3.5$ Volts
5. $V_2 = 0.2$ Volts
6. $V_3 = 0.5$ Volts
7. $V_A = 0.2$ Volts
8. $I_D = 2.5 \times 10^{-6}$ Amp (At 85°C)
9. $I_{c_{BO}} = 1.5602 \times 10^{-6}$ Amp (At 20°C)
10. $I_{1_{on}} = I_{2_{on}} = 57 \times 10^{-6}$ Amp
11. $I_{1_{off}} = I_{2_{off}} = 57 \times 10^{-6}$ Amp
12. $T_A = 85°C$
13. $T_R = 25°C$
14. $K = 0.3°C/MW$

SEE APPENDIX B-1 FOR DEFINITIONS

TABLE IV

NOMINAL CIRCUIT RESISTANCE VALUES

± Tolerance	R_1	R_2	R_K	R_B
0	28 580	28 580	134 200	146 200
5%	21 740	21 740	94 520	103 800
10%	14 480	14 480	55 550	61 190
15%	1 290	1 290	3 802	4 695

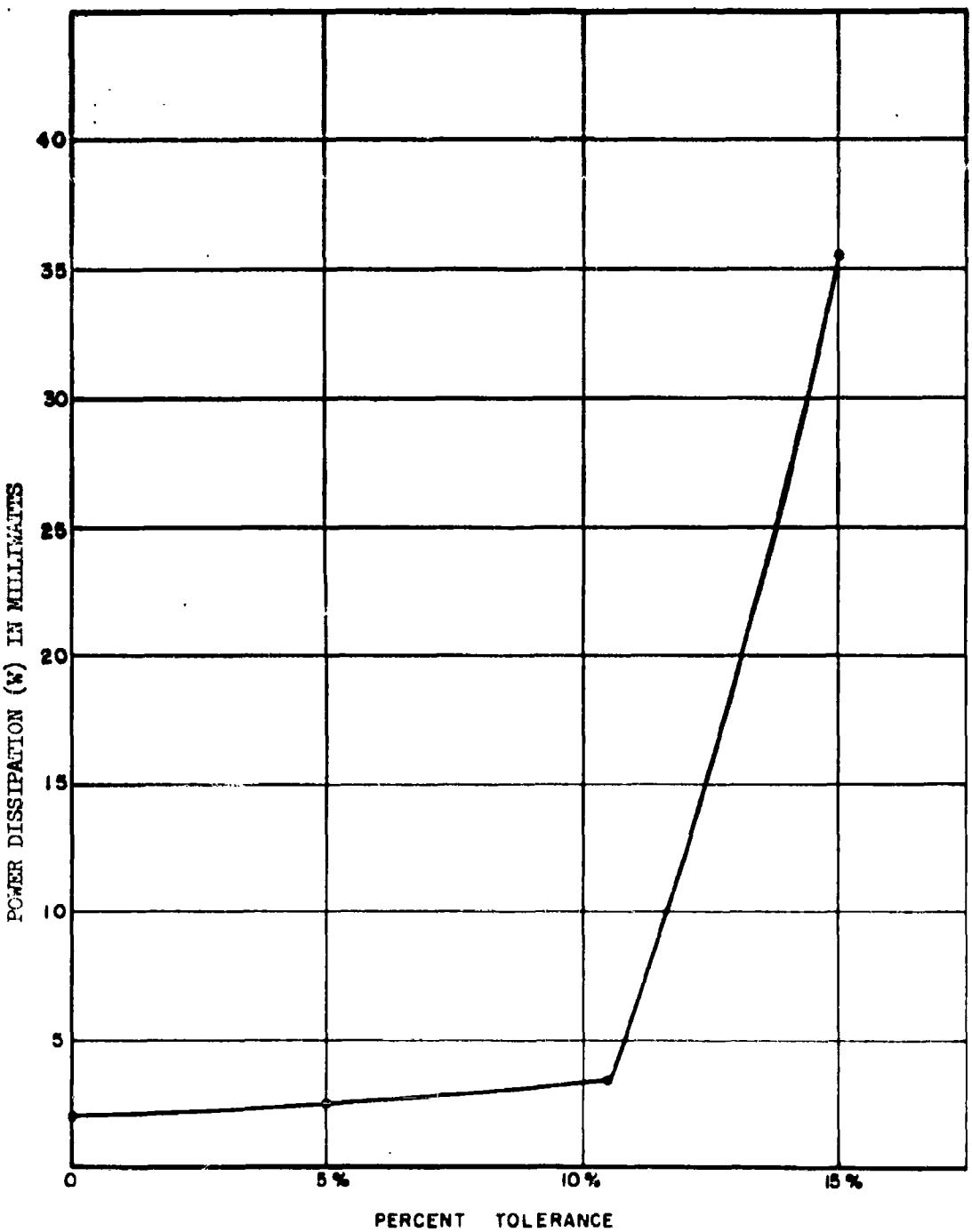


Figure 35 Power Dissipation vs. Percent Tolerance

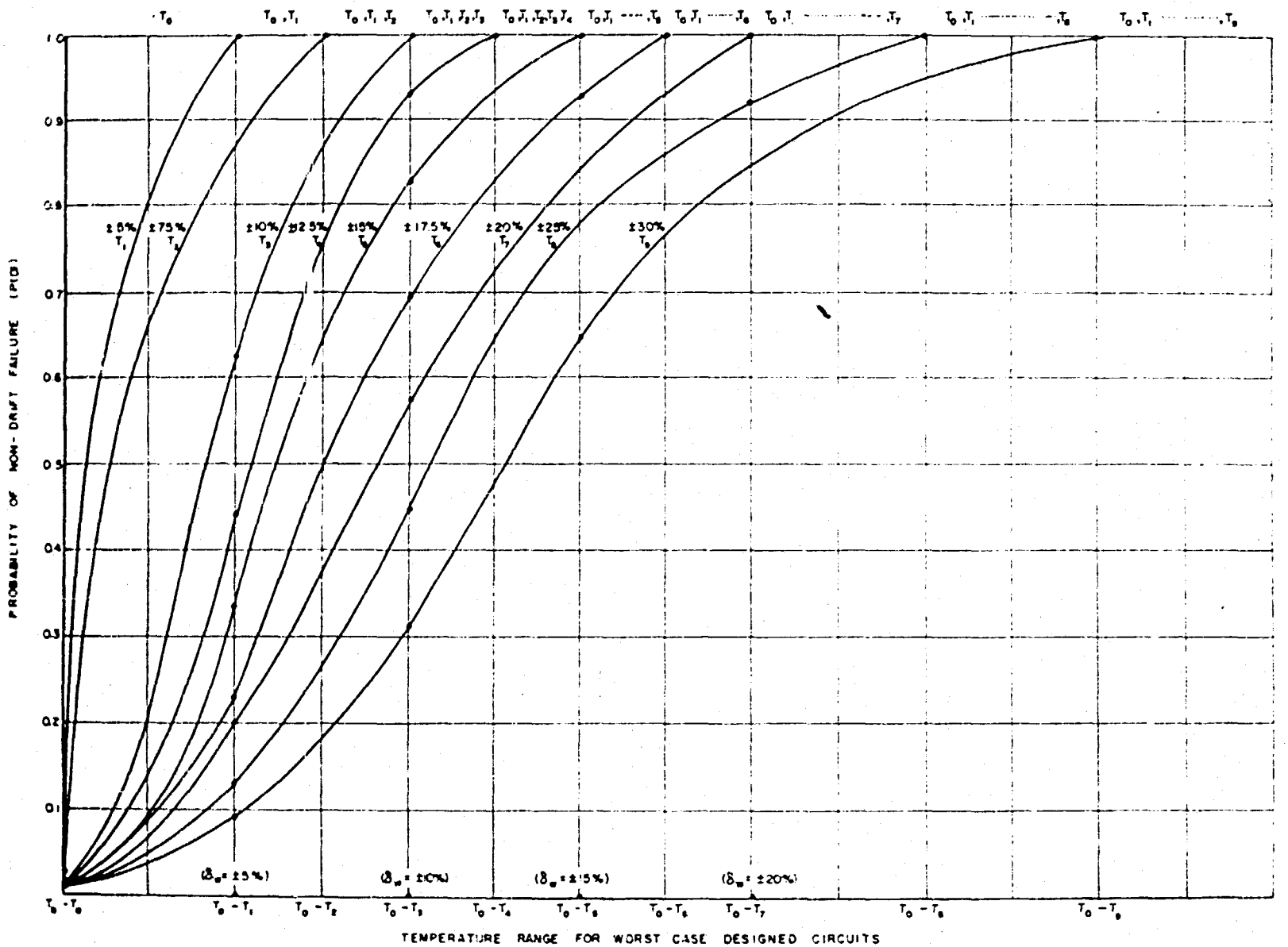


Figure 36. Probability of Non-drift vs. Temperature Range

Figure 36 shows the probability of non-drift failure vs temperature range or tolerance. Note that all of the circuits have P(D) = 1 for T_o or 0 tolerance. Moreover, all of the circuits have P(D) = 1 when tested with component distributions that do not deviate more than the initial circuit design tolerance. Thus, the values T_o, T_1 . . ., T_9 at the top of the graph indicate that a circuit is designed to hold up to the value of T_x indicated; the circuit designed for T_o - T_1 has P(D) = 1 up to T_1 while the circuit designed for T_o - T_3 has P(D) = 1 for T_o, T_1, T_2 and T_3.

3.3 Component Selection

As stated, the curves of Figure 36 indicate the probability of non-drift failure for the four worst case designed circuits when they are tested by a variety of component distributions. It was seen that the maximum reliability is attained for any of the circuits provided that the component tolerance values are less than or equal to the initial circuit design tolerance. Thus, the question of optimum tolerance remains up to this point unanswered. We answer this question in the material which follows.

Figure 37 shows four different types of typical component distributions where only positive tolerance values are shown in the Figure. Note that the best components are sold by Vendor A with a tolerance of $\pm$ 2% at 20°C with temperature dependence of the type A components given as 0.05%/°C. The worst components are sold by Vendor D with a tolerance of $\pm$ 15% at 20°C with the temperature dependence of the type D components given as 0.1%/°C. It is also pointed out that the cost of producing type A components is much greater than type B, C and D components.

Figures 35, 36 and 37 are used to construct Table V. In Table V we note further the superior quality of type A components. It is seen that if type A components are used in the 5% circuit, the circuit will function with P(D) = 1 from 20°C to 80°C. In the same circuit P(D) < 1 for type C and D components while P(D) = 1 only up to 20°C for the type B components.

3.4 Operating Temperature

It can be shown that the natural temperature of a circuit can be computed by some expression similar to

TABLE V

W IN MILLIWATTS

Circuit	Vendor	Temperature range where circuit will hold up. Corresponding to "T_o to T_x"	W in Watts
5%	A	20° to 80°	2.05
5	B	20° to 20°	2.03
5	C	None	2.03
5	D	None	2.03
10%	A	20° to 180°	3.1
10	B	20° to 95°	3.1
10	C	20° to 20°	3.1
10	D	None	3.1
15%	A	20° to 280°	35.5
15	B	20° to 170°	35.5
15	C	20° to 95°	35.5
15	D	20° to 20°	35.5

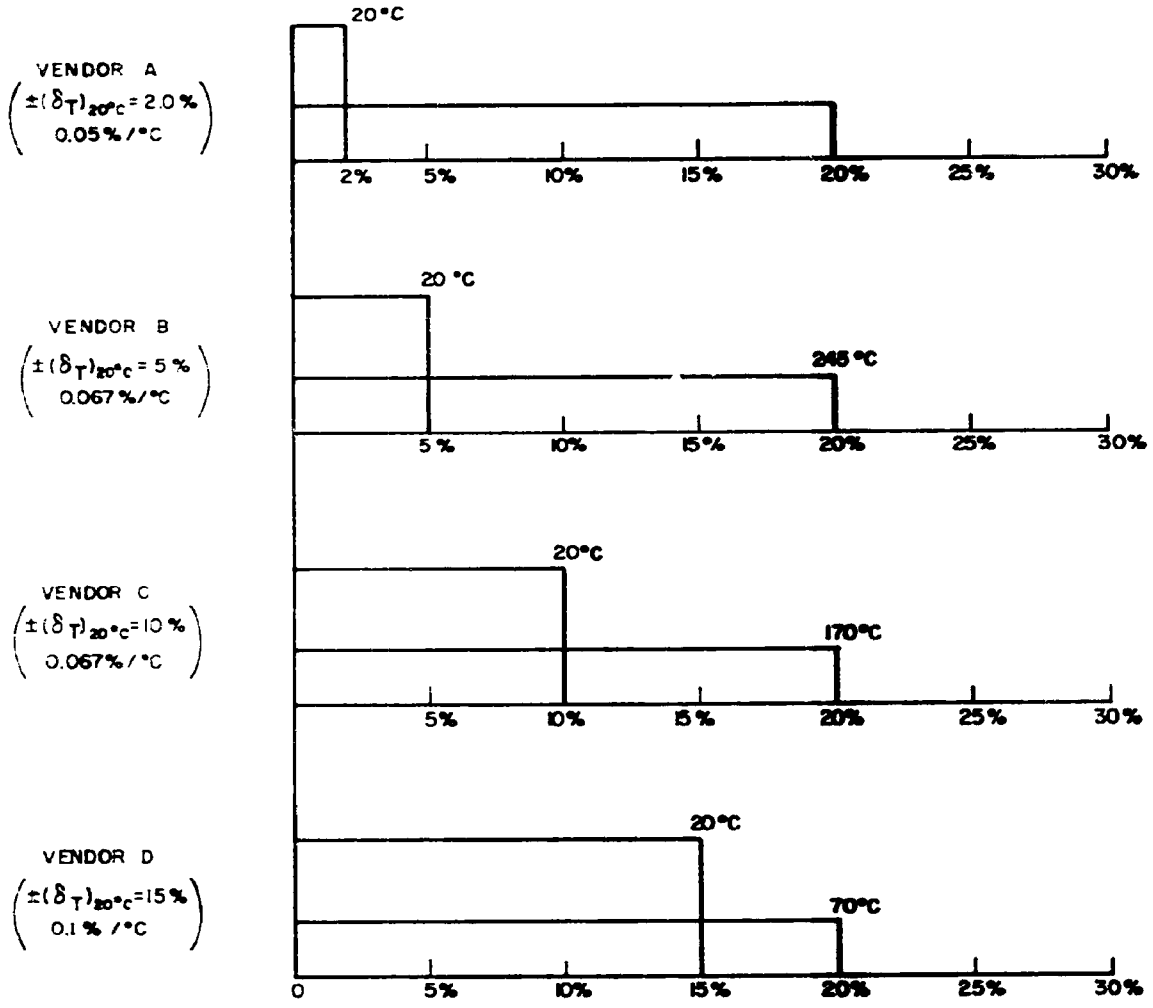


Figure 3?. Component Distributions of Four Vendors

$$T_{op} = W \cdot \text{constant} + T_o$$

where W = power dissipation

T_o = reservoir temperature

and the constant is dependent on insulation, conductivity or cooling arrangement. The curves of Figure 38 showing T_{op} vs T_o to T_x have been determined through utilization of equation 1, Table V and Figure 7. A typical point, say (75, 65.5), is determined as follows:

The point (75, 65.5) corresponds to the natural temperature of vendor C type components in a 15% circuit. The abscissa value, 75, corresponds to the difference between 20°C and 95°C for the type C components in the 15% circuit as seen in Table V. The ordinate value 65.5 is computed as

$$T_{op} = 35.5 \text{ MW} \cdot 1.0^{\circ}\text{C/MW} + 30^{\circ}\text{C}$$
$$= 65.5^{\circ}\text{C}$$

The 45° line of Figure 38 corresponds to $T_{op} = T_x$ (see Appendix B-1). Points intersecting the 45° line and to the right correspond to $P(D) = 1$ because they are equivalent to $T_{op} \leq T_x$. Points to the left of the 45° line correspond to $P(D) < 1$. Moreover, it is noted from the plotted curves that the value of $P(D)$ is a function of the type component used in a circuit, the power dissipation the reservoir temperature and the cooling effectiveness, noted by the constant C of Figure 38.

3.5 P(S) vs Tolerance (t = 0)

The previous information is now used to determine the probability of success, $P(S)$. As noted in Appendix B-1, $P(S) = P(D) \cdot e^{-\lambda t}$. It is first necessary to determine $P(D)$ at $t = 0$ corresponding to the particular value of operating temperature. It was shown in the previous section how to determine the operating temperature of a circuit. The operating temperature values and Figures 36 and 37 are used to determine $P(D)$ at $t = 0$. Table VI gives the computed values of T_{op}, the interpolated values of $P(D)$ at $t = 0$ and the failure rate values, λ, corresponding to the natural temperature.

A typical interpolated value of $P(D)$ is obtained as follows:
We note that the operating temperature for a type B component in a 5% circuit

TABLE VI

Tres	CKT #		A	B	C	D	A	B	C	D	A	B	C	D
20°C	5	$\pm\delta_T$	2.05	5.07	10.07	15.1	2.10	5.13	10.13	15.2	2.20	5.27	10.27	15.4
		P(D)	1.00	.9964	.6175	.336	1.00	.9928	.6125	.333	1.00	.9856	.6025	.327
			(T_{op} =21°, λ=3.54, C=½)				(T_{op} =22°, λ=3.58, C=1)				(T_{op} =24°, λ=3.66, C=2)			
	10	$\pm\delta_T$	2.08	5.1	10.1	15.155	2.15	5.2	10.2	15.31	2.31	5.4	10.4	15 62
		P(D)	1.00	1.00	.9973	.8202	1.00	1.00	.9946	.8118	1.00	1.00	.9892	.7950
			(T_{op} =21.55°, λ=3.56, C=½)				(T_{op} =23.1°, λ=3.62, C=1)				(T_{op} =26.2°, λ=3.73, C=2)			
	15	$\pm\delta_T$	2.89	6.18	11.18	16.775	4.78	7.37	12.37	18.55	6.55	9.73	14.73	22.1
		P(D)	1.00	1.00	1.00	.945	1.00	1.00	1.00	.86est	1.00	1.00	1.00	.82est
			(T_{op} =37.75°, λ=4.74, C=½)				(T_{op} 55.5°, λ=4.95, C=1)				(T_{op} 91°, λ=7.7, C=2)			

Computed T_{op}, Interpolated P(D), and λ

TABLE VI - CONTINUED

Tres	CKT #		A	B	C	D	A	B	C	D	A	B	C	D
30°C	5	$\pm\delta_T$	2.55	5.74	10.74	16.1	2.6	5.8	10.8	16.2	2.7	5.94	10.94	16.4
		P(D)	1.0	.96	.568	.303	1.0	.956	.564	.30	1.0	.95	.553	.41
			(T_{op} =31°, λ=3.84, C=½)				(T_{op} =32°, λ=3.88, C=1)				(T_{op} =34°, λ=3.96, C=2)			
	10	$\pm\delta_T$	2.58	5.77	10.77	16.155	2.65	5.87	10.87	16.3	2.8	6.07	11.07	16.6
		P(D)	1.0	1.0	.98	.778	1.0	1.0	.976	.76	1.0	1.0	.971	.743
			(T_{op} =31.55°, λ=3.86, C=½)				(T_{op} =33°, λ=3.92, C=1)				(T_{op} =36°, λ=4.04, C=2)			
	15	$\pm\delta_T$	3.38	6.84	11.84	17.75	4.275	8.05	12.05	19.55	5.55	10.43	15.43	23.0
		P(D)	1.0	1.0	1.0	.886	1.0	1.0	1.0	.838	1.0	1.0	.987	.80
			(T_{op} =47.75°, λ=4.46, C=½)				(T_{op} =65.5°, λ=5.5, C=1)				(T_{op} =101°, λ=8.8, C=2)			

Computed T_{op}, Interpolated P(D), and λ

Computed T_{op}, Interpolated P(D), and λ

TABLE VI - CONTINUED

Tres	CKT %		A	B	C	D	A	B	C	D	A	B	C	D
40°C	5	$\pm\delta_T$	3.05	6.4	11.407	17.10	3.10	6.47	11.47	17.2	3.2	6.61	11.61	17.4
		P(D)	1.0	.925	.5195	.270	1.0	.92	.515	.267	1.0	.912	.505	.361
			(T_{op} =41°, λ=4.24, C=½)				(T_{op} =42°, λ=4.28, C=1)				(T_{op} =44°, λ=4.36, C=2)			
	10	$\pm\delta_T$	3.075	6.44	11.44	17.15	3.35	6.54	11.54	17.30	3.3	6.74	11.74	17.6
		P(D)	1.0	1.0	.961	.715	1.0	1.0	.958	.706	1.0	1.0	.952	.695
			(T_{op} =41.5°, λ=4.26, C=½)				(T_{op} =43°, λ=4.32, C=1)				(T_{op} =46°, λ=4.44, C=2)			
	15	$\pm\delta_T$	3.89	7.53	12.53	18.77	4.78	8.72	13.72	20.55	6.55	11.1	16.1	24.1
		P(D)	1.0	1.0	1.0	.85	1.0	1.0	1.0	.843	1.0	1.0	.997	.79
			(T_{op} =57.7, λ=5.06, C=½)				(T_{op} =75.5°, λ=6.2, C=1)				(T_{op} =111, λ=10, C=2)			

NOTES: λ is in failures /.10^6 hrs., C is in °C/MW.

λ values for MIL-R-10509C Film Resistors (Reliability Stress Analysis for Electronic Equipment TR 59-416-1, RCA Report January 15, 1959)

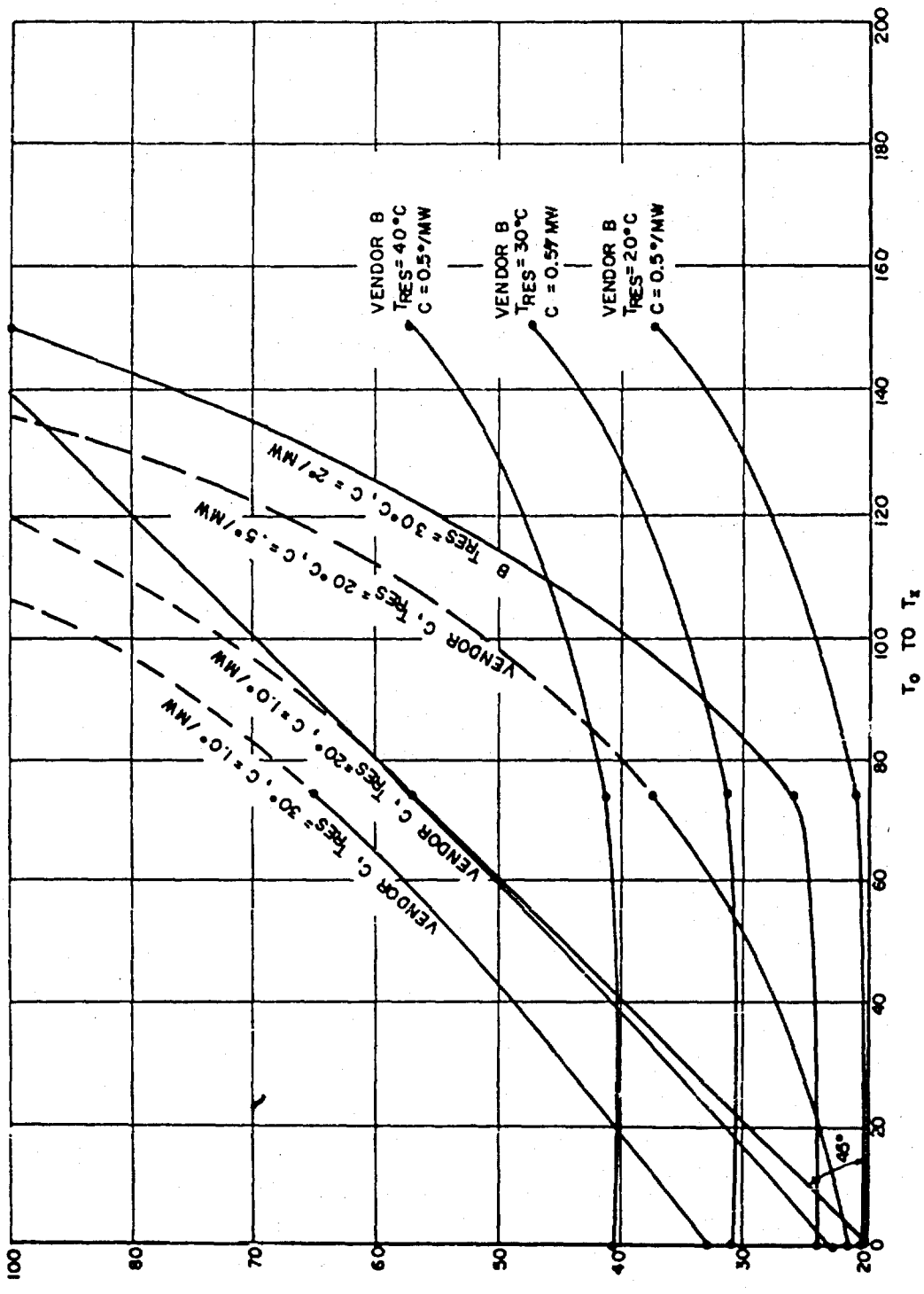


Figure 38. T_{op} vs. T_c to T_x

with C = 0.5°C/MW and $T_{Reservoir}$ = 20°C is 21°C. From Figure 37 the type B component at 21°C is seen to be 5.067%. From Figure 36 we note that a 5.067% component in a 5% circuit lies between P(D) = 1.00 and P(D) = .8642. Thus, the interpolated value is approximately P(D) = .9964.

Therefore, by utilizing the interpolated values of P(D), and the failure rate values of Table VI, the curves of Figures 39, 40, 41 were obtained. These curves show clearly the tolerances, that is the type component and circuit to use to maximize the reliability at time t = 0.

We note that type A components yield maximum reliability if used in either the 5, 10 or 15% circuits. Type B components yield maximum reliability if used in the 10 or 15% circuits. Type C components yield maximum reliability only in the 15% circuit. Whereas type D components yield poor reliability in all of the circuits. Thus, the optimum choice appears to be type A components in the 5% circuit. Note, however, that this choice is made purely on the basis of reliability and power dissipation. If cost is of consideration, then the choice would be type C components in a 15% circuit with poorer cooling corresponding to C = 2°C/MW.

3.6 Probability of Success vs Time

Previously, we have discussed the choice of component tolerances on the basis of the curves of Figures 39, 40 and 41 for P(S) at time t = 0. At t>0 the choice may be different due to the increase of failure rate as a function of power dissipation and temperature.

In Figures 42, 43, 44, 45, and 46 we show different curves of P(S) vs time. It should be noted in particular that someof these curves show cross over points; a curve starting at a lower value of P(S) intersects a curve starting at a higher value of P(S). Thus, of vital importance in the selection of component tolerance is the time of operation.

Figure 42 shows P(S) vs time for the various type components when used in a 5% circuit. Note that the choice of component type is clearly the type A components. In Figure 43 the choice of component type would be the type A or B components; choose type B components for the 10% circuits for cost reasons. In Figure 44 the choice of component type wouldbe the type A, B, or C

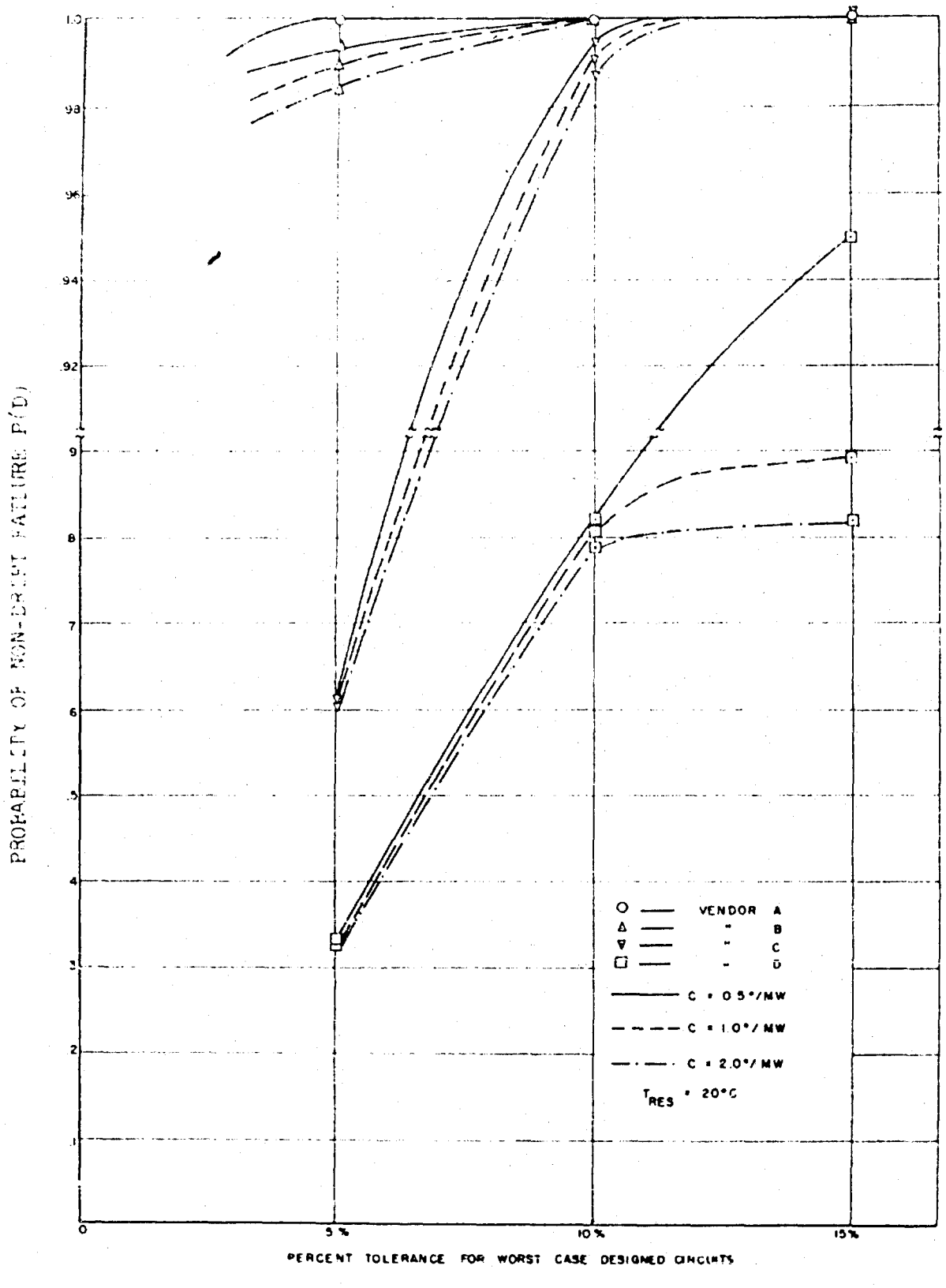


Figure 30. Probability of Success vs. Percent Tolerance

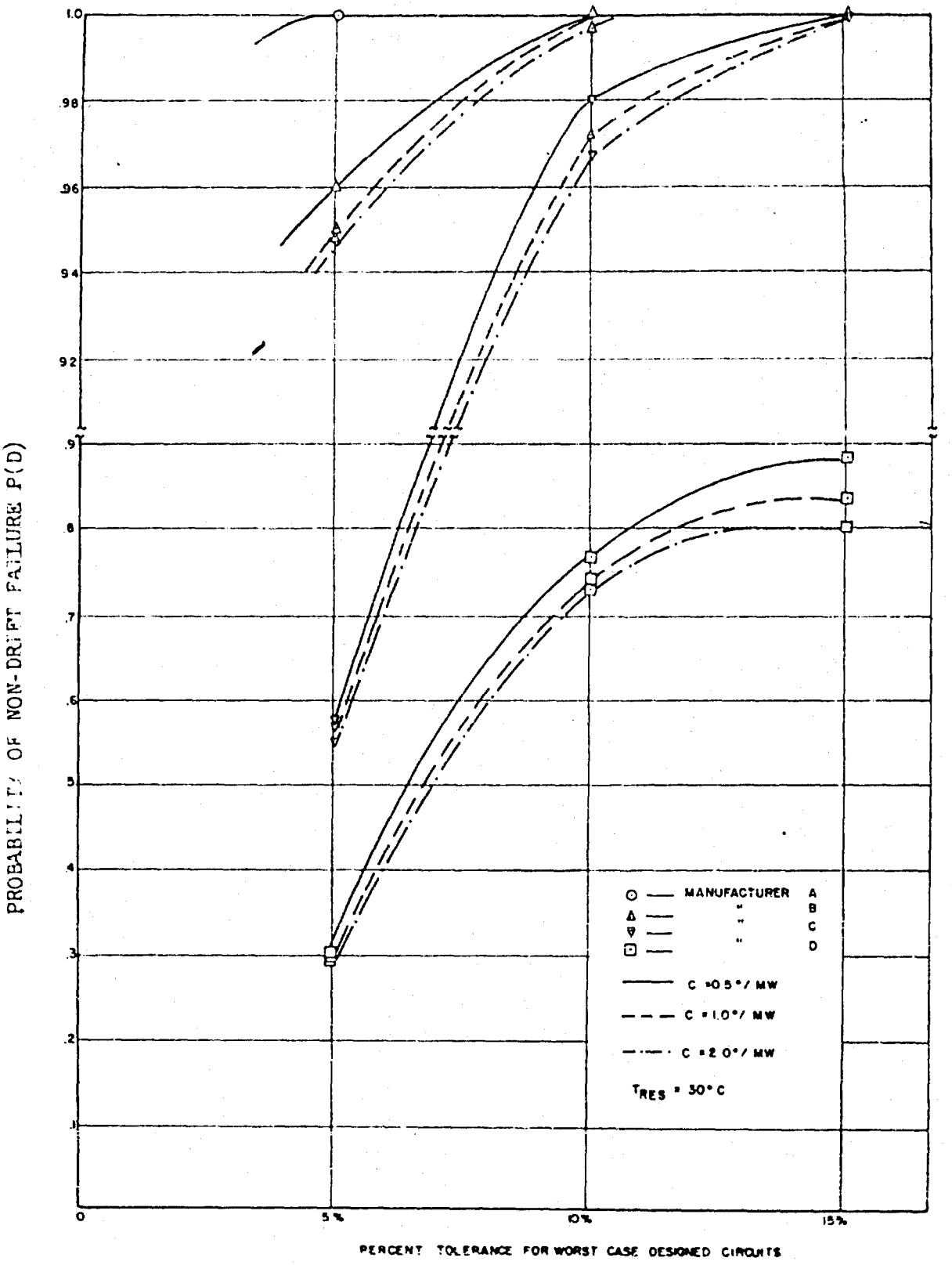


Figure 40. Probability of Success vs. Percent Tolerance

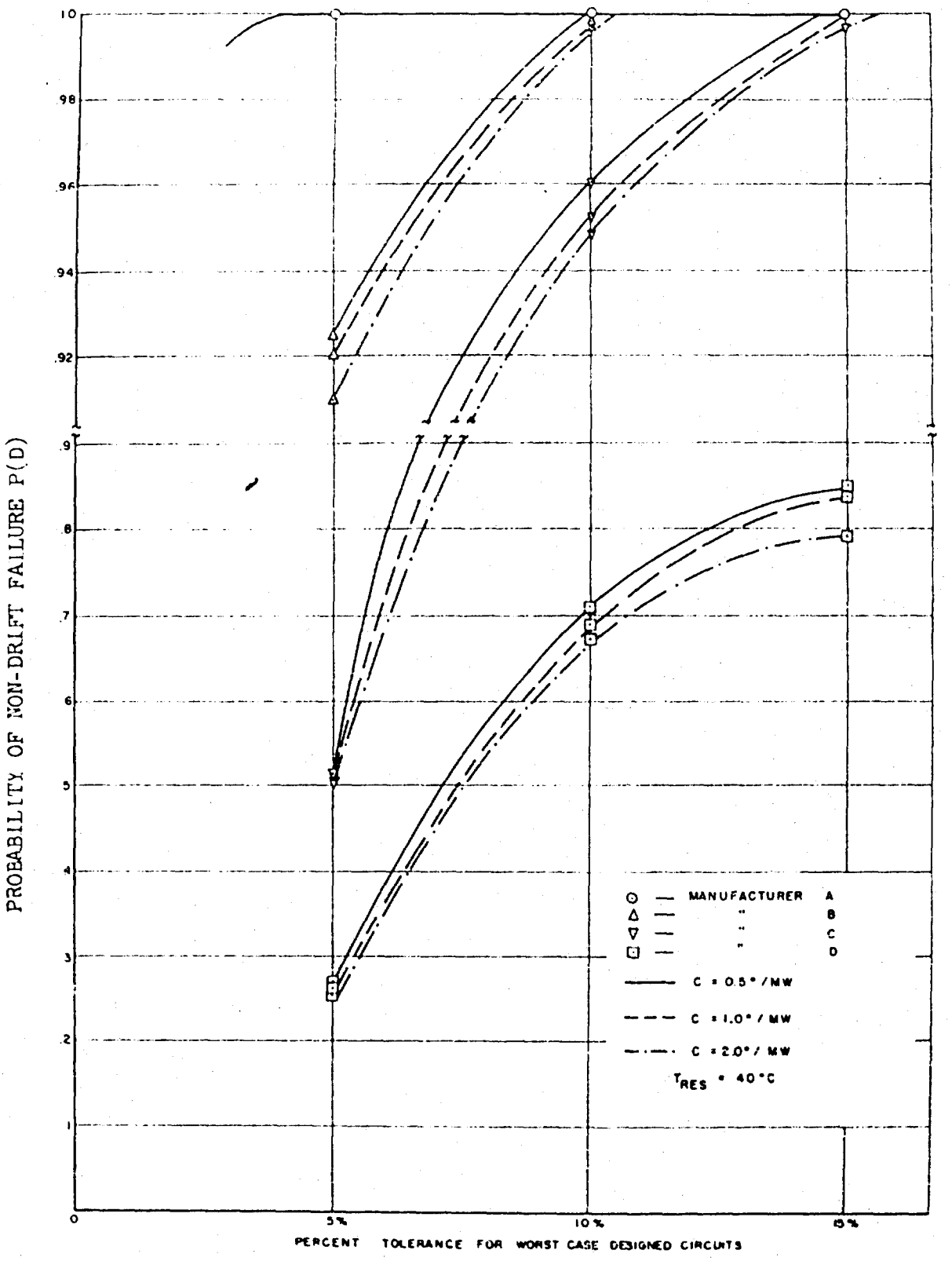


Figure 41. Probability of Success vs. Percent Tolerance

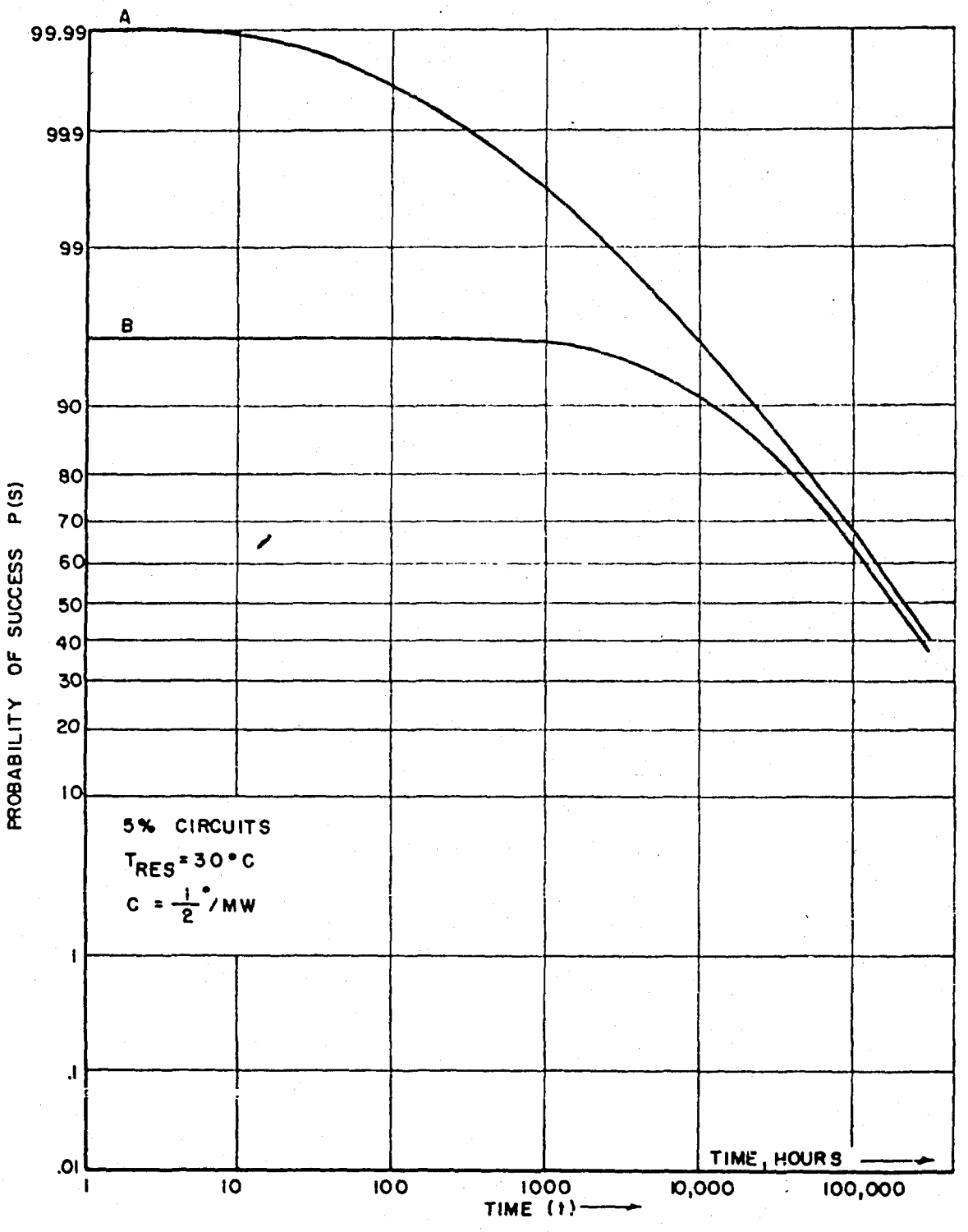


Figure 42. Probability of Success vs. Time

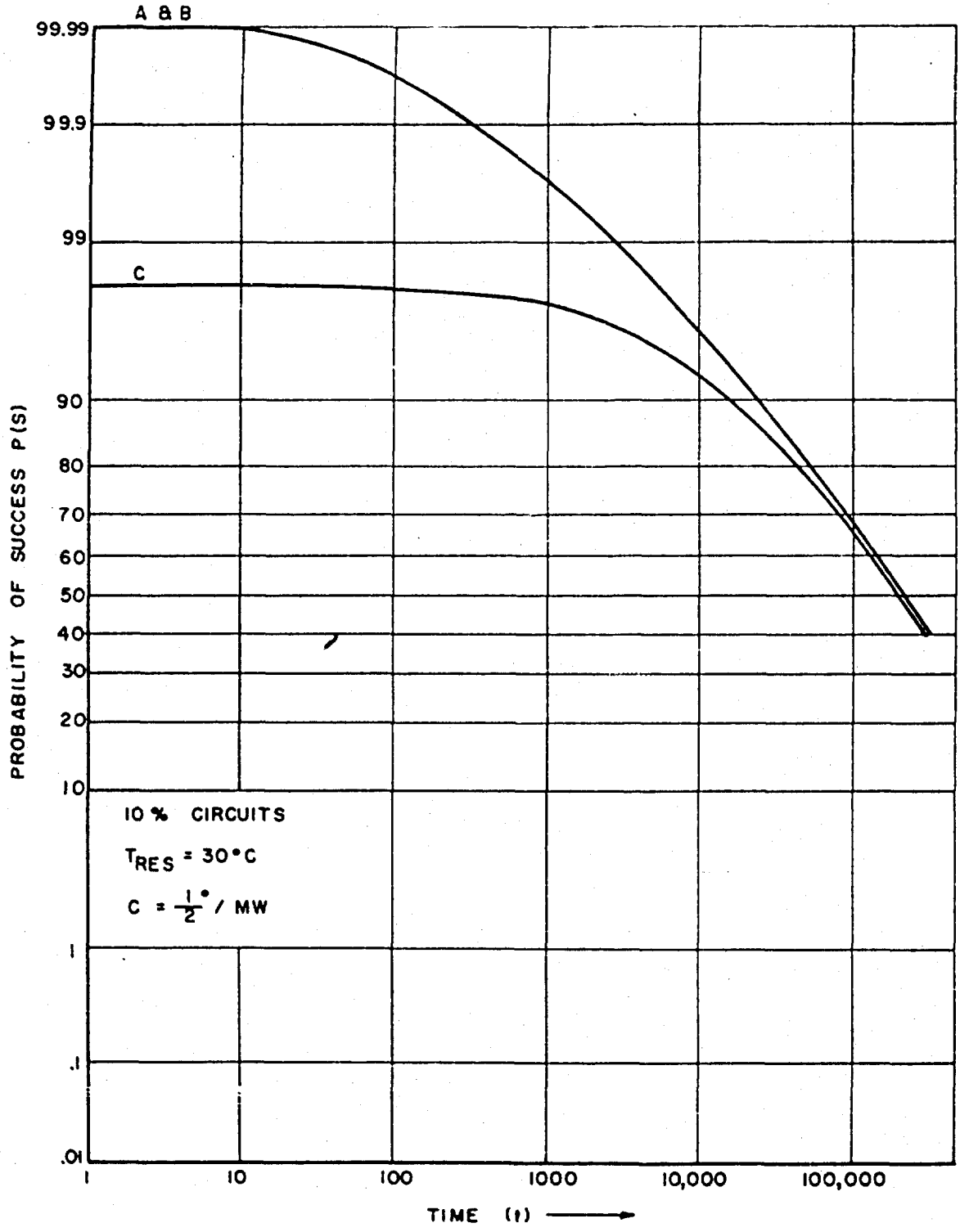


Figure 43. Probability of Success vs. Time

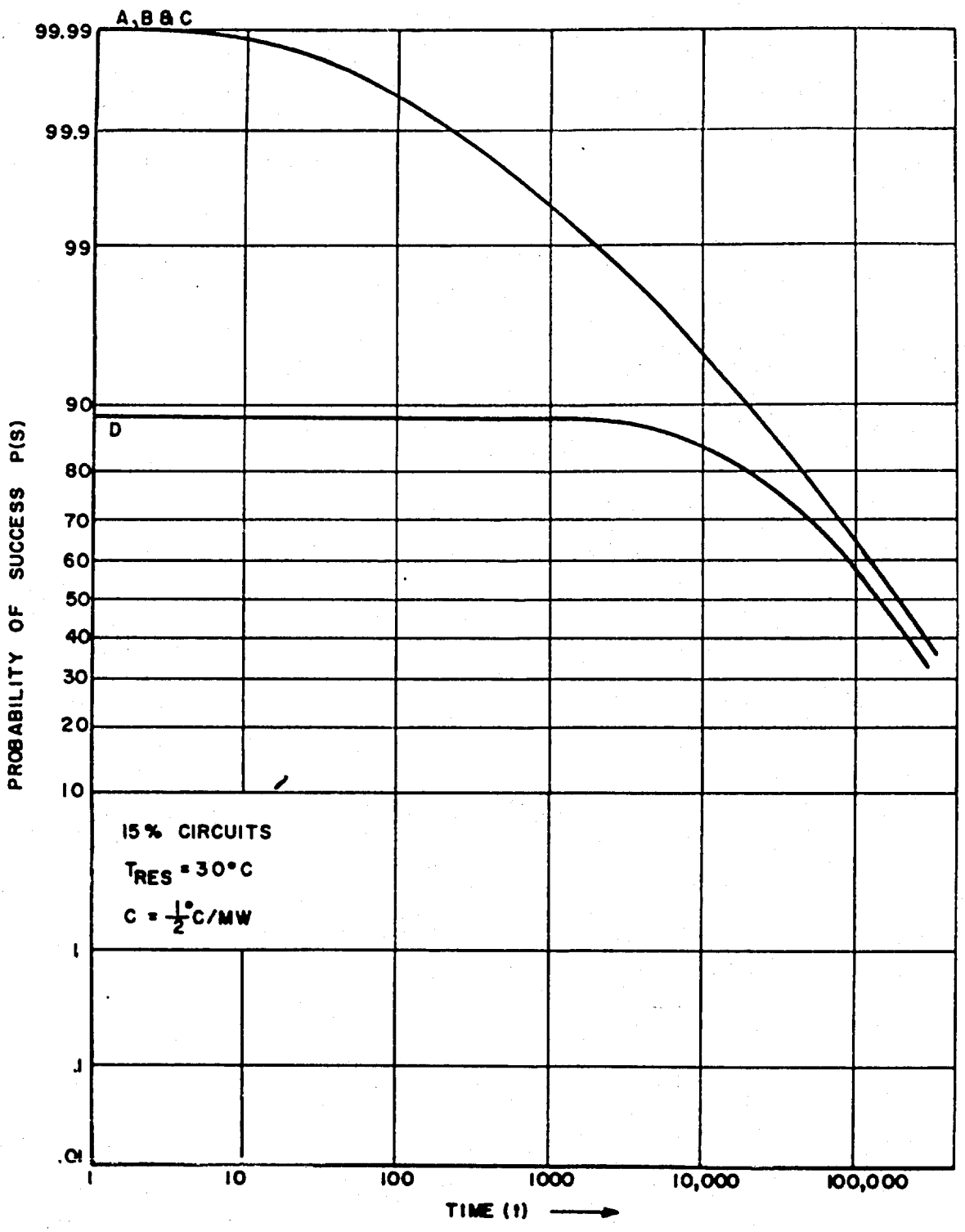


Figure 44. Probability of Success vs. Time

components; choose type C components for the 15% circuits for cost reasons.

Figures 45 and 46 yield, however, a different picture for selection purposes note that definite intersections exist. These intersecting points indicate that if it is required to operate the circuits for long periods of time then these intersections should be considered. Note that the type D components (C = 1/2¢/MW and C = 1¢/MW) in the 15% circuit have larger P(S) values at t > 30,000 hrs.and t > 54,000 hrs. than the type A or B components at C = 2¢/MW. Previously there was no indication in the results to consider the use of type D components for maximum reliability. It is evident that the curves showing type D components in the 15% circuit have a low value of P(S) initially, P(S) ≈ 0.84 to 0.88. If one is willing to pay the cost of selecting out and eliminating approximately 22 per cent of the circuits built with these components through some type of "burn in" tests, then it would be of advantage to use the type D components in the 15% circuit which would now start initially at P(S) = 1 and decay at a much slower rate than the circuit using type A or B components.

In Figure 46 we show a comparison between type B components in a 15% circuit and type C components in a 10% circuit. An intersection occurs at approximately 50,000 hours but the difference between the two beyond this point appears insignificant because there is little difference in the rate of decay.

In Figure 47 we show a comparison between type A, B and C components in a 15% circuit and type B components in a 5% circuit. Note here that the only difference is the reservoir temperature, T_{RES}. The intersection occurs at approximately 2,500 hours, a very short time. The significance here is that the optimum tolerance selection procedure is also applicable at short times.

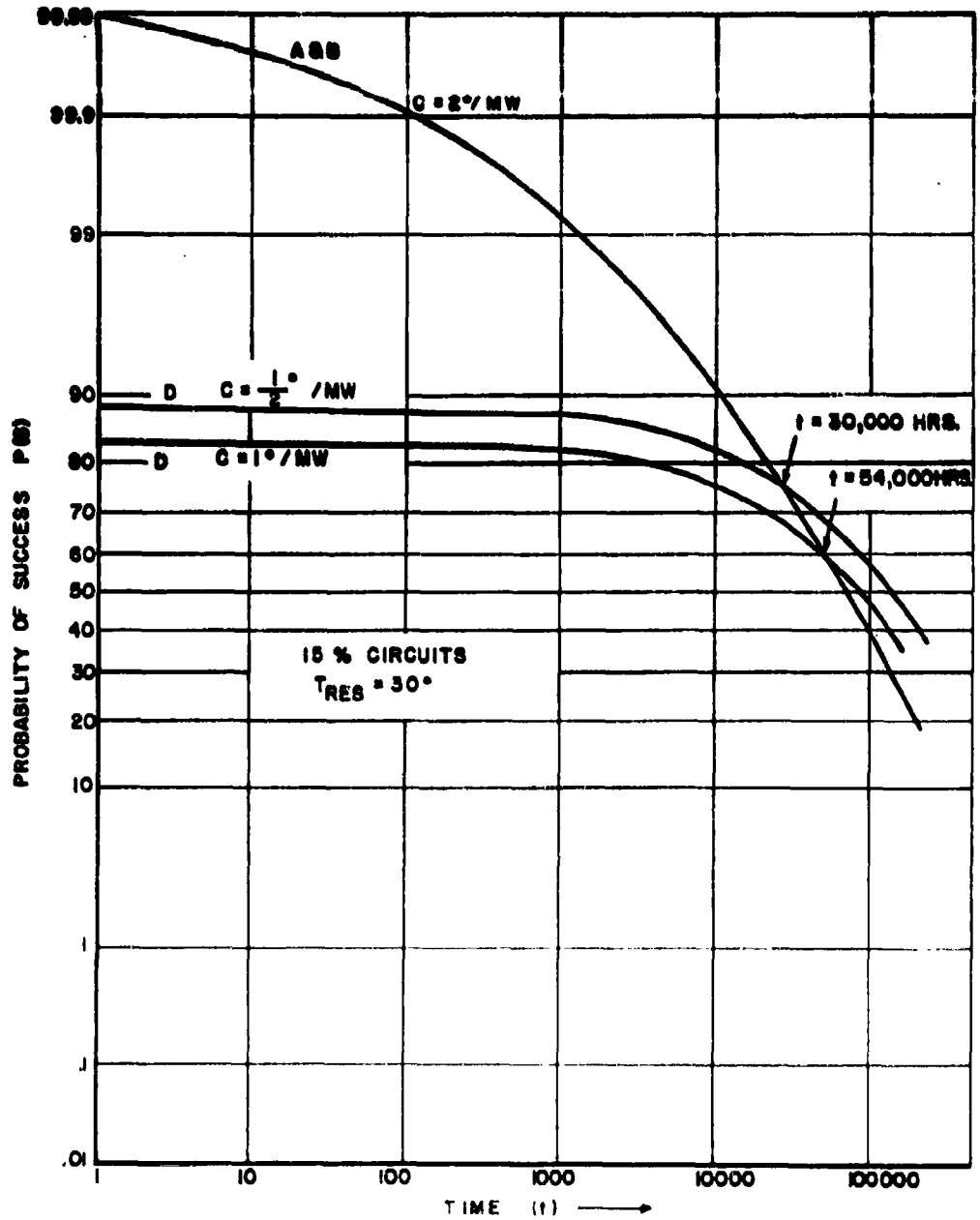


Figure 4b. Probability of Success vs. Time

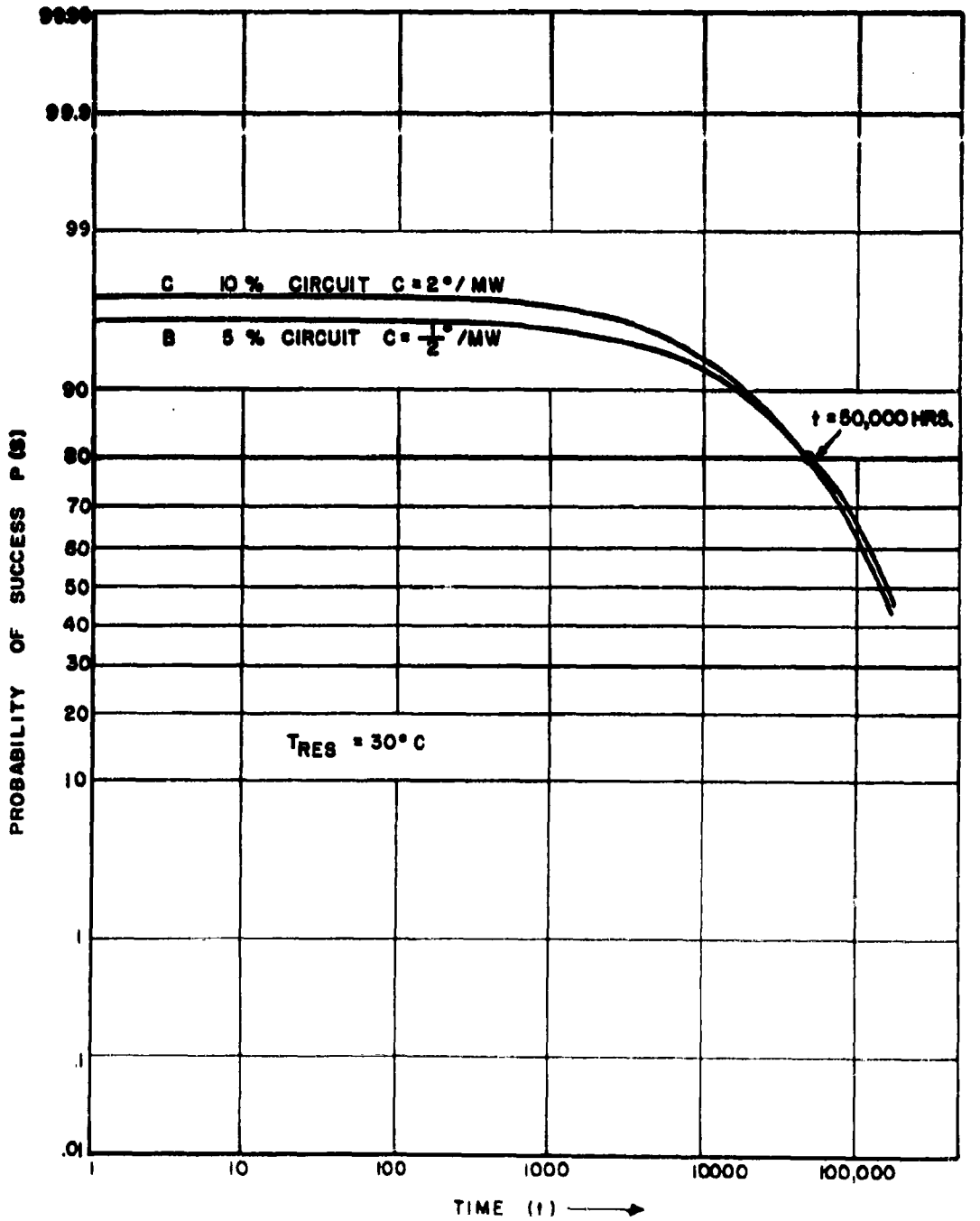


Figure 4. Probability of Success vs. Time

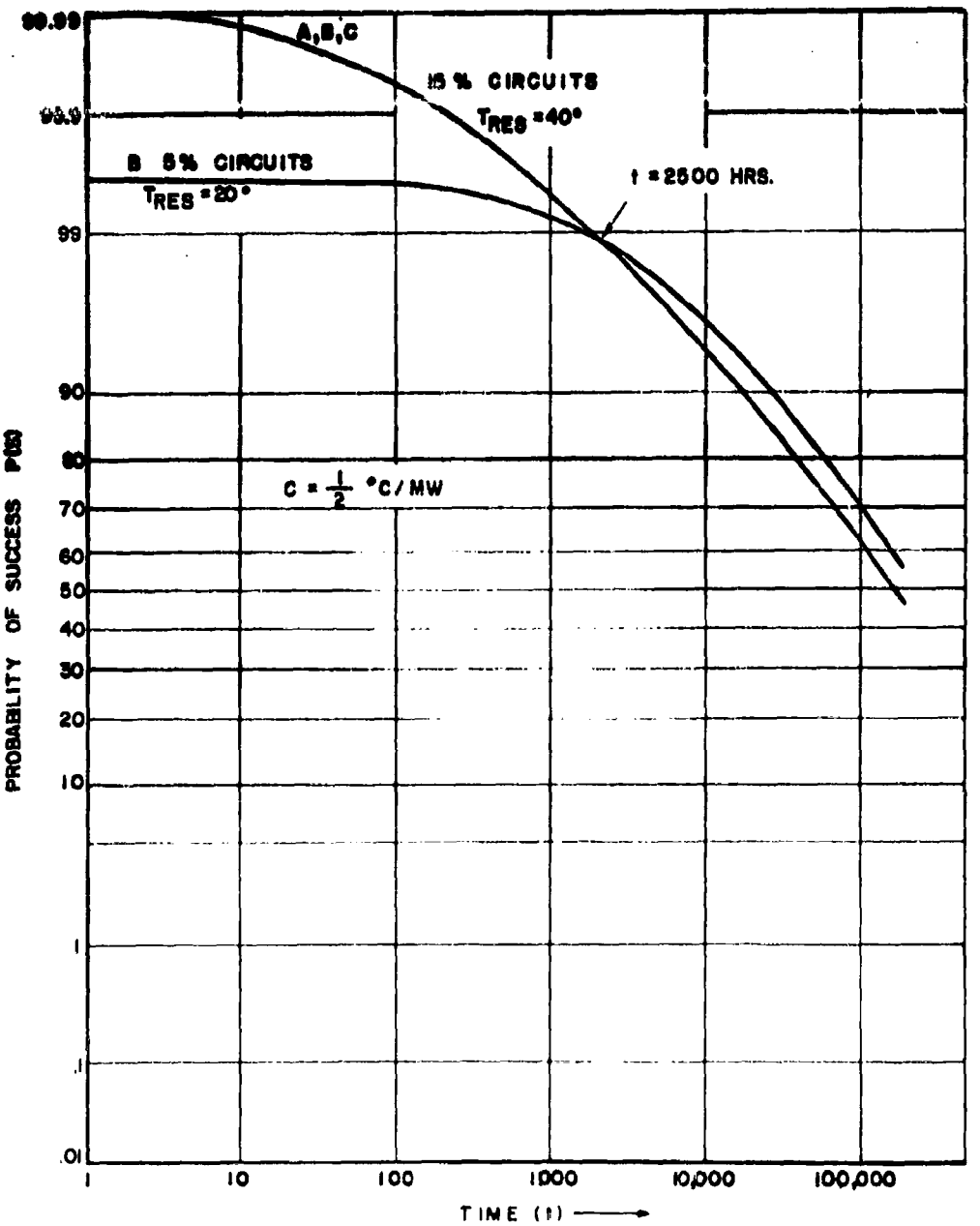


Figure 4. Probability of Success vs. Time

3.7 Summary of Procedure for Finding Optimum Design

(a) It is assumed that all component and parameter distributions are known. As the distributions are assumed truncated it is possible to worst case design circuits which will show no failure due to component drift, $P(D) = 1$, for temperature ranges "T_o to T_o", "T_o to T_1", etc. Such circuit designs are listed in Table IV.

A worst case designed circuit (described by a set of nominal component values) designed for some temperature range, say "T_o to T_4", is determined exclusively by: the design method (see Appendix B-2) and the distributions of the vendors' components in the temperature range T_o to T_4. To make the comparisons of the 4 vendors' products easy to follow, the distributions shown in Figure 37 were assumed. $\pm 10\%$ component variation will then correspond to the distributions found in the temperature range 20° to 95° for all vendor B components. Notice that $\pm 10\%$ is also the distribution of all vendor A's components in the range 20° to 180° etc., as shown in Table V.

(b) Next the power dissipation W, is computed for each circuit, see Figure 35 or Appendix B-1, Figure 2. The average power dissipation, W, depends exclusively on the nominal values of the circuit resistors.

(c) The operating temperature, T_{op}, is computed for each circuit, by the expression $T_{op} = W \times C +$ Reservoir Temperature, see Figure 38 or Appendix B-1, Figure 3 and Table VI. The two constants, the thermal resistance C°/mW and the reservoir-temperature (which is usually the ambient temperature), are significant only in so far as they relate the circuit power-dissipation W to the natural temperature of the circuit. The expression: $T_{op} = W \times C +$ reservoir temperature, was discussed in Part 3.4 and Appendix B-1, Part (g). T_{op} is used twice, see part (d) and (e) below.

(d) The catastrophic failure rate λ is determined for each circuit. λ depends exclusively on T_{op} and the curves shown in Figure 5 of Appendix B-1. The curves will, in general, be different for different vendors' products. The λ values are listed in Table VI.

(e) P(D), the probability of no failure due to component drift, is found for each circuit by interpolation for T_{op}, see Part 3.5.

For a given circuit, designed for say "20° to 70°" and vendor D's components, P(D) depends exclusively on T_{op} and the curves on Figure 36 or Appendix B-1, Figure 1. Figures 39, 40 and 41 show how P(D) is influenced by T_{res} and C since $T_{op} \quad W \times C + T_{res}$.

The curves shown in Figure 38 and Appendix B-1, Figure 4 are helpful in showing whether or not T_{op} for a circuit falls in the temperature range, "T_o to T_x", for which the circuit was designed. When $T_{op} \leq T_x$ it means that $P(D) = 1$. When $T_{op} > T_x$, P(D) must be found by interpolation.

(f) P(S) is the probability of satisfactory operation at time t. P(S) is computed for each circuit as $P(S) = P(D)\ e^{-\lambda t}$. Figures 42 to 47 illustrate P(S) for the different circuits as a function of time for different vendors' components, reservoir temperatures and thermal conductivities. From such figures it is possible to decide which circuit, component type, and cooling system should be used.

3.8 Conclusions

In Section IV, Part B and Appendix B-1 an answer was given to the problem: how can $P(S) = P(D) \times e^{-\lambda t}$ for a circuit or system by optimized for a given time or time interval? P(D) is the probability of no failure due to component drift. $e^{-\lambda t}$ is the probability of no catastrophic failure at time t . P(S) is the probability of satisfactory operation at time t .

The optimum P(S) at a given time is found by comparing corresponding points on curves such as those in Figures 42 to 47. If the average P(S) over some time interval is of interest, it is necessary to use integration as shown in Appendix B-1, Figure 7.

The answer to the above problem is given in terms of:

(1) some temperature range , "T_o to T_x",

(2) the type of components which should be used,

(3) the thermal resistance C^o/mW and the reservoir-temperature, which is usually the ambient temperature. The two constants are significant only in so far as they relate the circuit power-dissipation W to the operating temperature of the circuit by the expression: T_{op} = W x C + reservoir temperature.

Some relationships between the more important factors will now be reviewed.

(a) A worst-case designed circuit (described by a set of nominal component values) designed for some temperature range, say "T_o to T_4" is determined exclusively by: the design method and the distributions of the vendors' components in the temperature range T_o to T_4.

(b) The average power dissipation, W, of a circuit depends exclusively on the nominal values of the resistors.

(c) The catastrophic failure rate λ depends exclusively on T_{nat} and the curves Appendix B-1, Figure 5. The curves will, in general, be different for different vendors' products.

(d) For a given circuit, designed for say "20° to 70°" and vendor D's components, P(D) depends exclusively on the operating temperature, T_{op}, and the curves on Appendix B-1, Figure 1.

(e) The initial distribution at room temperature (called $\delta\ (T)_{20^\circ}$ in Figure 37) of any vendors' components can be made as narrow as desired by selection. The selected components will still have the same temperature coefficient and λ-curves (see Appendix B-1, Figure 5) as before. A narrow component distribution will make the resistor values in worst case designed circuits larger and the power dissipation, W, smaller. If the resistor-distributions are reduced from ± 20% to ± 5% all resistor values are increased by at least 15%, as may be seen by inspection of the design inequalities, likewise the power dissipation will decrease by 15% or more. As the operating temperature, T_{op}, depends on the product of power dissipation and thermal resistivity, W x C, it is seen that narrowing the resistor distribution from ± 20% to ± 5% is equivalent to reducing the thermal resistivity, C, by 15% or more.

Paragraphs (a) to (e) show the relationships which determine the trade-off possibilities. During the second year of this program it is planned to study quantitatively the relative merits of the various trade-offs.

C. TERMINAL PARAMETER MEASUREMENTS

The problem of consideration is the evaluation of circuit performance with emphasis given to the evaluation of circuit sensitivity to component variations. The specific problem arises as a result of functional or integrated microelectronic circuitry in which the components are inaccessible for measurement following fabrication. Unconventional component variations are the primary concern where for a particular circuit design the complete fabrication occurs in one or several steps. Independent of the number of steps the final unit consists of an integrated structure which can be analyzed only through the aid of terminal measurements.

Thus, we have the following items given:

1. a fabricated microelectronic circuit with a limited number of available terminals for test purposes
2. the circuit design and specifications

The problem is to:

1. make measurements to determine circuit parameter values
2. make an analysis of the circuit performance and predict the probability of circuit failure or verify the accuracy of the fabrication technique

There are two general approaches that may be taken to evaluate the circuit from terminal parameter measurements. First, one can treat the circuit as a "black box" and simply determine what it can do without regard to the internal component state of the circuit. The problem is analogous to characterizing a transistor from measurements without developing an equivalent circuit that would be useful over a variety of operating conditions. This approach requires a large number of measurements on a given circuit in order to accurately predict its performance for a variety of operating conditions (i.e., frequency, temperature, etc.).

Secondly, one may determine the nominal values of the circuit components by measurements at available terminal points.[1] Knowledge of how the component values vary with environment would thus allow prediction of circuit performance. This approach roughly corresponds to the problem of determining an equivalent circuit for a transistor. With the original component design values, the circuit can then be analyzed to determine its performance capability.

The second approach seems more useful since it can be done with relatively few measurements compared to the "black box" approach. One assumes, however, that it is possible to measure all of the circuit component values. If not, then some combination of the two approaches may be necessary. Use will be made largely of the second approach for this study with consideration of other methods when it is necessary.

Consideration has been given to the limitations imposed on measurement and analysis procedures by given circuit configurations. Some factors considered were:

a. the circuit is operating at nominal design and voltage current levels

b. the components of the circuit are connected as the design requires but no voltage are applied

c. measurements can be made only at available terminal points

d. measurements impose no damaging stresses on components

e. the conventional circuit design is known

f. active devices are conventional or unconventional

g. the circuit is fabricated in parts or as a complete unit

h. accuracy of measurement

---

[1] R.S. Berkowitz, "Conditions for Network-Element-Value Solvability," IRE Transactions on Circuit Theory, Volume CT-9, March 1962, pp 24-29

i. data is available on how components vary with operating conditions and environments

j. data is available on how components vary with age

k. data is available on component failure rates

Item (a) is analogous to the condition of establishing circuit performance capability by the "black box approach". The primary difficulty is the problem presented in not knowing the individual component values. For example, one could determine the performance of the circuit at that point in time by measurement, but prediction of performance for some future time would be based entirely on the probability of catastrophic failure for the circuit. This is so because one component, say a resistor, could have its value very close to the tolerance point for failure of the circuit without being detected in measurement.

Item (b) essentially allows the application of voltages and currents to the circuit with resulting measurements of individual component values. It permits flexibility in measurement such that one is not limited to particular measurement techniques. Since individual component values are measurable with a certain degree of flexibility, this method as stated previously has been adopted for the study. The remaining items have served the purpose of establishing a general philosophy to follow in defining specific techniques.

It is pointed out that for some circuits the determination of all component values, particularly active drive parameter values, may be impossible. If this occurs, then one has to resort to a combination of the techniques presented here and others.

The material of Appendix C-1 gives the results of effort conducted to determine the applicability of the method pointed out here. These investigations were carried out on a general purpose amplifier and a flip-flop circuit.

Experimental Results

Terminal parameter measurements have been made on three manufacturer's type flip-flop circuits that are being fabricated currently in microelectronics form. The flip-flop circuits were chosen for analysis because of their complexity and due to the fact that they are utilized in large numbers. These circuits are designated in the following material as:

1. flip-flop - Manufacturer A
2. flip-flop - Manufacturer B
3. flip-flop - Manufacturer C

1. FLIP-FLOP CIRCUIT (MAN. A)

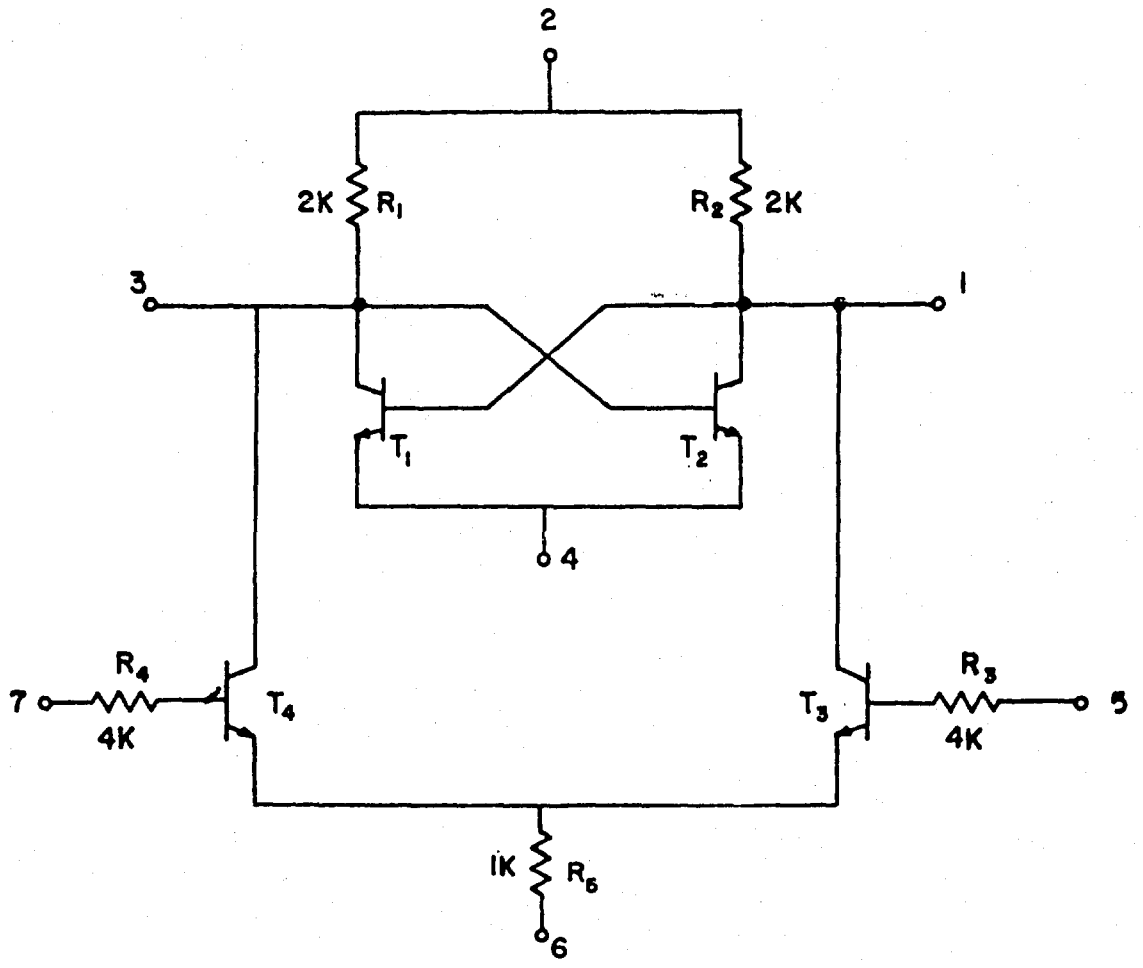


Figure 48. Flip-flop with 7 Available Terminals.
Component values as indicated.

a. Passive Circuit Components

A convenient approach is to consider the transistor as two back-to-back diodes as pointed out in Appendix C-1.

(1) Determination of R_1 and R_2

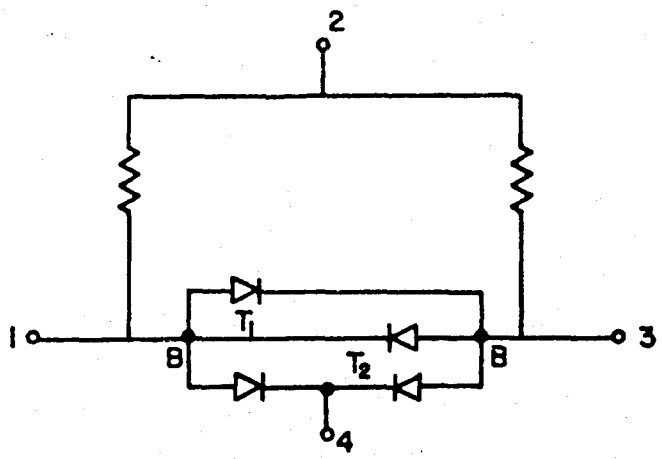


Figure 49. Equivalent Circuit

To eliminate error in measurement due to loop current through junctions between terminals (1)-(3), terminals (1)-(3) should be balanced by applying the same positive potential to them and connecting terminal (2) to ground. The values of R_1 and R_2 are obtained by measuring the currents through terminals (1)-(2) and (3)-(2) and computing R_1 and R_2

$$R_1 = \frac{E}{I_1} \quad , \quad R_2 = \frac{E}{I_2}$$

True value of $R_1 = R_2 = 2K$

Measured value of $R_1 = R_2 = 2K$

Note: Connecting terminal (4) to ground and terminals (5) and (7) to a positive potential gives balance between terminals (1)-(3). If the balance

cannot be obtained, it is an indication of emitter junction breakdown of T_1 or T_2.

(2) Measurement of R_3

An a-c measurement of voltage and current between terminals (5)-(1) with collector junction of T_3 forward biased gives the value of R_3.

True value $R_3 = 4K$

Measured value $R_3 = 4K$

(3) Measurement of R_4

The procedure is identical to the determination of R_3. The ac measurement between terminals (7)-(3) with the collector junction of T_4 forward biased gives the value of R_4.

True value $R_4 = 4K$

Measured value $R_4 = 4K$

(4) Measurement of R_5

An ac measurement between terminals (5)-(6) with the emitter junction of T_3 forward biased yields the value of $R_3 + R_5$.

True value $R_5 = 1K$

Measured value $R_5 = 1K$

b. Important Transistor Parameters

(1) Determination of β_o and the common emitter cutoff frequency of T_3:

β_o is the common emitter short circuit current gain. Apply the design voltage between terminals (1)-(6) through a 100 Ω resistor, to approximate an ac short circuit at the output. Drive the circuit between terminals (5)-(6) with an ac generator in series with a 100 k resistance

to approximate small signal current source. β_o is then given

$$\beta_o = \frac{i_c}{i_b} = \frac{V_2/100}{V_1/100K}$$

at 1000 cps and a one volt-input the measurement yields

$$\beta_o = 45$$

β_o measured with the transistor test set "Owen" type 210A gave a $\beta_o = 48$. By increasing the frequency to a value where $\beta = \beta_o/\sqrt{2}$ we find f_β:

$$f_\beta = 120 \text{ kc}$$

(2) Determination of β_o and the common emitter cutoff frequency of T_4

The procedure is identical to the determination of β_o and f_β of T_3.

Design voltage between terminals (3)-(6)
Drive voltage between terminals (7)-(6)

$$\beta_o = 42$$

β_o measured with the transistor test set "Owen" type 210A gave a $\beta_o = 44$.

$$f_\beta = 110 \text{ kc}$$

(3) Determination of β_o of T_1

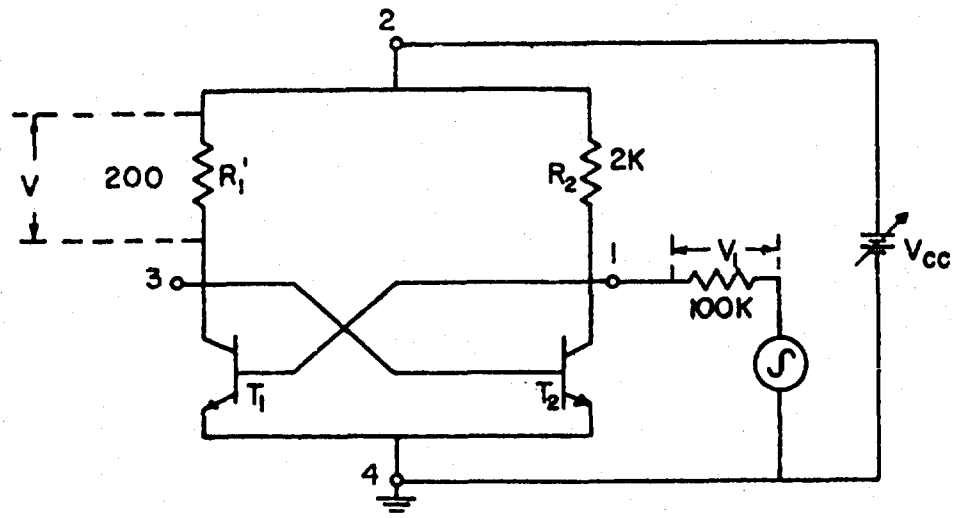


Figure 50. Circuit for Determining β_o of T_1

To approximate ac short circuit at the output, connect a low valued resistance between terminals (2)-(3). With the circuit of Figure 3, β_o is obtained as follows:

we see from the figure that

$$\beta_o = \frac{i_c}{i_b} = \frac{V_2/200}{V_1/100K}$$

over the linear region β_o measured was

$$\beta_o = 35$$

β_o measured with the transistor test set "Owen" type 210A gave a $\beta_o = 37$.

(4) Determination of β_o of T_2

The procedure is identical to the determination of β_o of T_1.

Design voltage between terminals (2)-(4)

Drive voltage between terminals (3)-(4)

$R_2^1 = 200$

Measured $\beta_o = 32$

β_o measured with the transistor test set "Owen" type 210A gave a $\beta_o = 33$.

(5) The determination of other transistor paramters as C_E, C_c is obtained by the methods outlined in Appendix C-1.

2. FLIP-FLOP CIRCUIT (MAN. B)

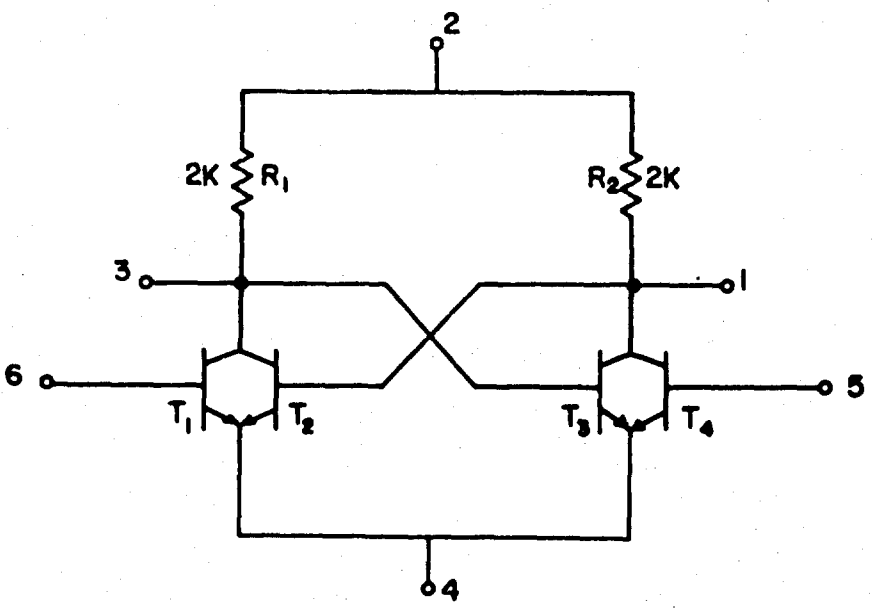


Figure 51. Flip-flop with 6 Available Terminals
Component values as indicated.

a. Passive Circuit Components

(1) Determination of R_1 and R_2

The procedure is identical to the determination of R_1 and R_2 in the Flip-flop circuit of man. A.

b. Important transistor parameters

(1) Determination of β_o of T_2 and T_3

The procedure is also identical to the determination of β_o of T_1 and T_2 in the flip-flop circuit of man. A.

(2) Determination of β_o of T_1

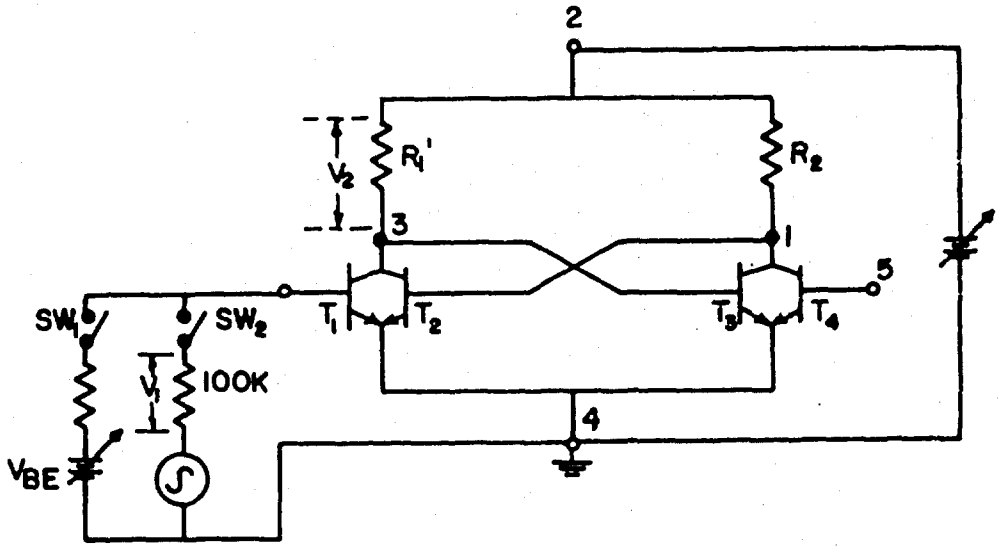


Figure 52 .Circuit for Determination of β_o of T_1

The circuit of Figure 5 is used in this measurement.

The method to measure β_o of T_1 is the following:

a. Apply design voltage such that T_2 is in saturation and T_3 not conducting.

b. V_{CE} of T_1 and T_2 should be approximately 0.4 Volt

c. Connect a low value resistor between terminals (2)-(3).

d. For the above conditions the increase in collector current due to conduction of T_1 (SW1 closed) is I_c or T_1.

e. Drive T_1 (after closing SW2) between terminals (6)-(4) with an ac generator in series with a 100 k resistance.

f. β_o is given by

$$\beta_o = \frac{V_2/200}{V_1/100K}$$

measured $\beta_o = 42$

β_o measured with the transistor test set "Owen" type 210A gave a $\beta_o = 44$

(3) Determination of β_o of T_4

The procedure is identical with that of determining β_o of T_1.

$$R_2^1 = 200\ \Omega$$

$$\beta_o = \frac{V_2^1/200}{V_1^1/100K}$$

measured value of $\beta_o = 40$

β_o measured with the transistor test set "Owen", type 210A gave a $\beta_o = 43$.

3. FLIP-FLIP CIRCUIT Man. C

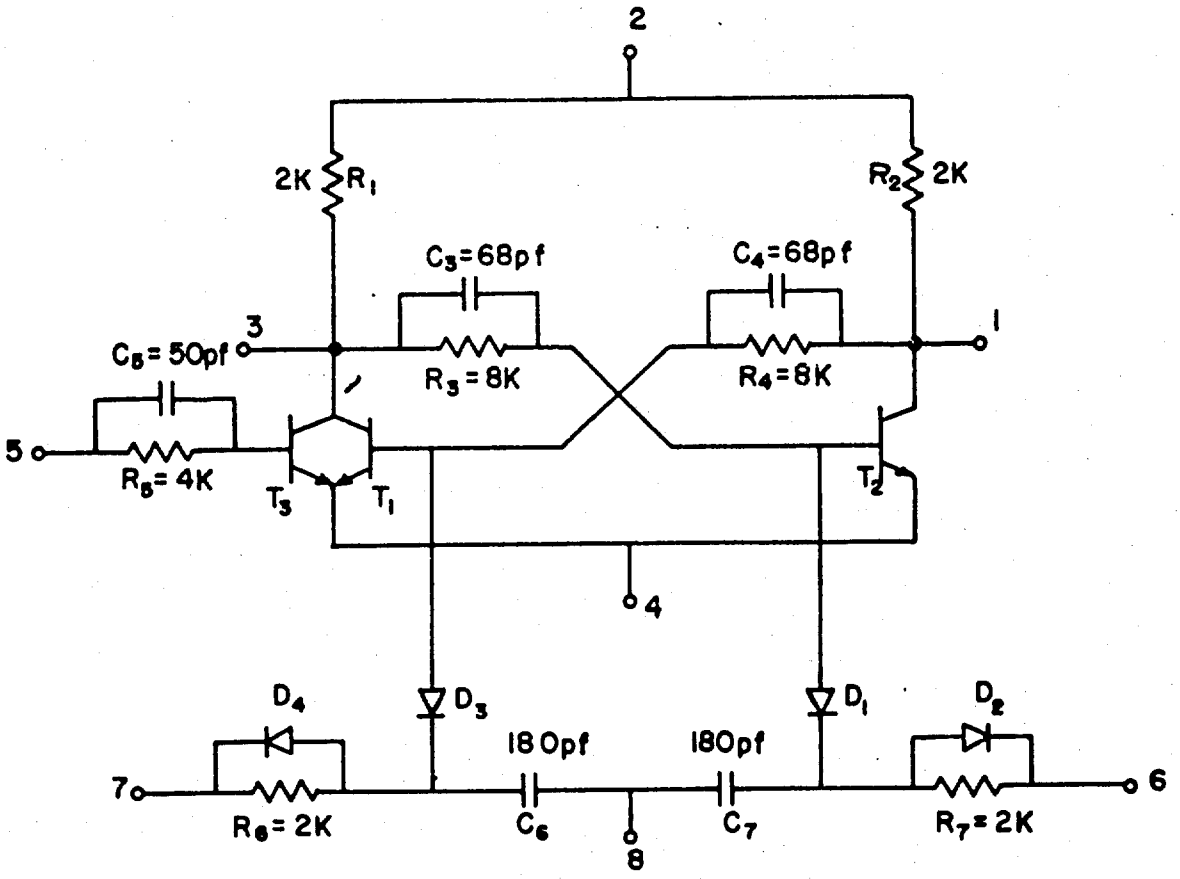


Figure 53. Flip-flop with 8 Available Terminals
Component values as indicated.

a. Passive Circuit Components

(1) Determination of R_1 and R_2

The method of measurement as identical with that applied to A and B.

Measured value $R_1 = R_2 = 2K$

True value $R_1 = R_2 = 2K$

(2) Determination of R_3

An ac measurement between terminals (3)-(6) with the diodes D_1 and D_2 forward biased yields the value of R_3

Measured value $R_3 = 8K$

True value $R_3 = 8K$

(3) Determination of R_4

An ac measurement between terminals (1)-(7) with diodes D_3 and D_4 forward biased yields the value of R_4.

Measured value $R_4 = 8K$

True value $R_4 = 8K$

(4) Determination of C_3

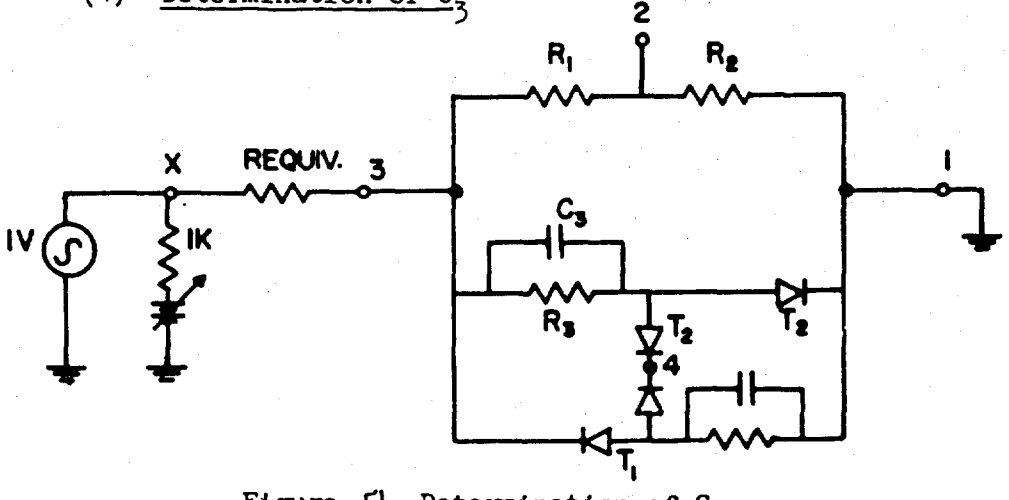


Figure 54. Determination of C_3

With the circuit of Figure 54 C_3 is obtained as following:

(a) $Reqv = \frac{(R_1 + R_2)R_3}{R_1 + R_2 + R_3}$

(b) apply on ac voltage of 1 V rms and 500 cps between terminals (x) - ground

(c) bias the circuit such that $v_{31} = 0.5\ v_{x1}$

(d) increase the frequency of the ac generator to a frequency where the value of $V_{31} = \frac{0.5\ V_{x1}}{\sqrt{2}}$. Keep the amplitude of the input signal at 1 V rms.

(e) compute the value of C_3 from equation:

$$C = \frac{2}{2\ \pi\ f\ Reqv.}$$

Measured value of C_3 = 69 μμf

(5) Determination of C_4

The method is identical with that of determination of C_3 with terminals (1) and (3) interchanged.

Measured value of C_4 = 72 μμf.

(6) Determination of R_5

An ac measurement between terminals (5)-(3) with collector junction of T_3 forward biased yields the value of R_5.

Measured value of R_5 = 4K

True value R_5 = 4K

(7) Determination of C_5

The value of C_5 is obtained by means of an impedance measurement between terminals (5)-(3), with the collector junction of T_3 forward biased.

The impedance between terminals (5)-(3) is

$$Z = R + jx = r_D + \frac{1}{\frac{1}{R_5} + j\omega c} =$$

$$V_D + \frac{R_5}{1 + \omega^2 R_5^2 C_5^2} - j\ \frac{\omega R_5^2 C_5}{1 + \omega^2 R_5^2 C_5^2}$$

at low frequencies ($f < 20$ Kc)

$$\omega^2 R_5^2 C_5^2 << 1$$

so that the impedance expression becomes

$$Z = r_D + R_5 - j\omega R_5^2 C_5.$$

The bridge balances for

$$Z = 4200 + \frac{1}{j}\,50$$

This leads to the value of $C_5 = 50$ pf.

(8) Determination of R_6 and C_6

An admittance measurement between terminals (7)-(8) with diode D_4 reverse biased yields the values of R_6 and C_6.

The bridge balances for

$$Y = \frac{1}{2K} + j\omega\, 180 \text{ pf.}$$

(9) Determination of R_T and C_T

The method is identical with that of determining R_6 and C_6

Measure between terminals (6)-(8) with diode D_2 reverse biased.

The bridge balances for

$$Y = \frac{1}{2K} + j\omega\, 180 \text{ pf.}$$

The true values were:

$$R_6 = R_7 = 2K$$

$$C_6 = C_T = 180 \text{ pf.}$$

3-b. Important Transistor Parameters

(1) Measurement of β_o of T_3

Connect a 220 Ω resistance in parallel with R_1 and a 220 Ω resistance in parallel with R_2. Apply a dc voltage between terminals (2)-(4). The state of the flip-flop is such that T_1 is not conducting and T_2 is conducting. Forward bias the emitter junction between terminals (5)-(4) with a low dc-voltage. Apply a signal between terminals (5)-(4) through a 100 k resistance. The β_o of T_3 is given by:

$$\beta_o = \frac{i_c}{i_b} = \frac{V_2/200}{V_1/100K}$$

The measured value $\beta_o = 43$

The value measured with the transistor test set "Owen" type 201A was $\beta_o = 45$.

(2) Measurement of β_o of T_1

Connect a 220 Ω resistance in parallel of R_1 and one in parallel with R_2. Apply a dc voltage between terminals (2)-(4). Connect a variable resistance (25 K) between terminals (1)-(4). Bring the flip-flop to a state where T_1 is conducting and T_2 is not conducting. Connect a resistance (7K) between terminals (6)-(4), to prevent the flip-flop from changing states during adjustment of the variable resistance. Adjust the resistance and the D-C voltage such that the collector junction of T_1 will be slightly reverse biased. Apply an ac signal between terminals (7)-(4) through a 100 k resistance. (The diodes D_3 and D_4 are forward biased.) The β_o of T_1 is given

$$\beta_o = \frac{V_2/200}{V_1/100K} .$$

The value measured $\beta_o = 45$

The value found with the transistor test set "Owen" type 201A is $\beta_o = 45$

(3) Measurement of β_o of T_2

The method is identical with that of measuring β_o of T_1. Connect in parallel with R_1 and R_2 220 Ω resistances. Apply a dc-voltage between terminals (2)-(4). Connect a variable resistance (25K) between terminals (3)-(4). Connect a resistance (7K) between terminals (7)-(4). Apply an ac signal between terminals (6)-(4) through a 100 k resistance.

The β_o of T_2 is given

$$\beta_o = \frac{V_2/200}{V_1/100K} .$$

The value measured $\beta_o = 37$. The value found with the transistor test set "Owen" type 201A is $\beta_o = 40$.

D. ADJUSTABILITY

1. General Adjustability Considerations

Adjustability is often a desirable feature in electronic equipment. Two rather distinct classes of system adjustability are (1) adjustment of basic system functions such as gain, bandwidth, etc., and (2) adjustment of critical component values located, for example, in tuned amplifiers. A rather unique class of tunable band-pass filters, referred to as "digital filters", was singled out for special attention in the area of adjustability. A brief summary of digital filter characteristics is given in the following section.

2. Digital Filter Characteristics

The digital filter consists of a bank of N low pass networks whose input and output terminals are sequentially commutated at a frequency f_o. Three outstanding characteristics of the digital filter are (1) the center frequency can be easily varied, (2) the bandwidth can be easily varied and (3) extremely narrow bandwidths (less than 1 cps) are achievable.

The operation of the digital filter can be visualized as follows. Consider a low-pass network whose voltage transfer function is characterized, for example, by the response shown in Figure 55. Under certain band limiting constraints which were previously discussed, it is possible to incorporate this low-pass network into the digital filter and thus produce the band-pass characteristic shown in Figure 56. The center frequency f_c can be varied without affecting the bandwidth, or conversely, the bandwidth can be varied without affecting the center frequency. It should be noted that, except for a scale factor, the shape of the band-pass characteristic is the same as the shape of the low-pass characteristic. In particular, if the low-pass network has a cutoff frequency f_1, the band-pass filter will have cutoff frequencies at $f_o \pm f_1$. As a consequence, it is possible to generate extremely narrow-band filters. For example, a single low-pass RC section could easily be built with a 3 db cutoff frequency less than 1 cps. When this RC section is used in the

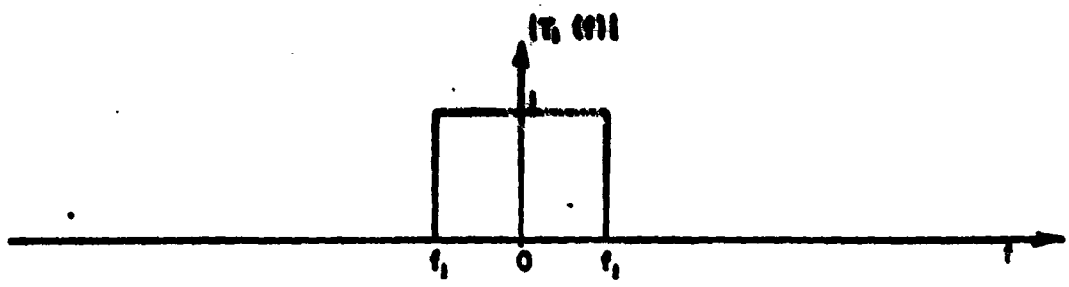


Figure 55. Low-pass Voltage Transfer Function

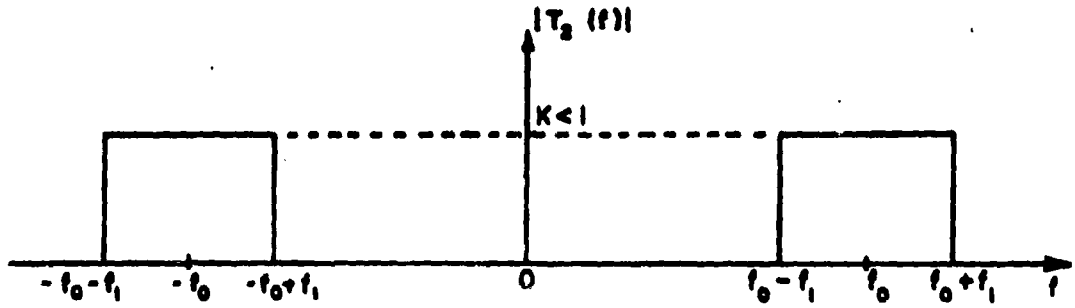


Figure 56. Band-pass Voltage Transfer Function

digital filter, the pass band response will be down 3 db at a frequency less than 1 cps away from the center frequency.

The basic theory describing the digital filter was discussed in the Second Quarterly Report. In the Third Quarterly Report, a laboratory implementation of the digital filter was described, and the digital filter transfer function was evaluated at 1600 cps where operation as a tone selector might take place. The digital filter can also be operated at center frequencies in excess of one megacycle, and the present report will describe some of the operating characteristics at high frequencies.

3. High Frequency Digital Filters

The prime limitation associated with high frequency operation of a digital filter stems from an inability to generate sufficiently good switching functions. More specifically, considering the basic digital filter shown in Figure 57, the problem is to implement the sequential opening and closing of the four switches. At any particular time, one and only one switch should be closed. Furthermore, all the switches should close for the same length of time. In practice, each of the four switches can be replaced by a transistor, and digital circuitry can be designed to generate the switch operating signals. At high frequencies, problems arise because a transistor switch cannot change states instantaneously. This shortcoming is significant both in the generation of the switching waveforms and in the actual operation of the switch.

The switching waveforms employed in the previously described digital filters were generated by combining the outputs from two cascaded flip-flops through resistor-diode logic. This technique is practical at low frequencies, but at high frequencies, the circuit time delays become intolerable. When time delays are negligible, this system operates as shown in Figure 58 in which the representative waveform AB is positive whenever both A and B are positive. However, when rise times, fall times and storage times become significant, AB will no longer have the desired shape. Improved operation at high frequencies can be obtained by generating the switching waveform in a shift register. This

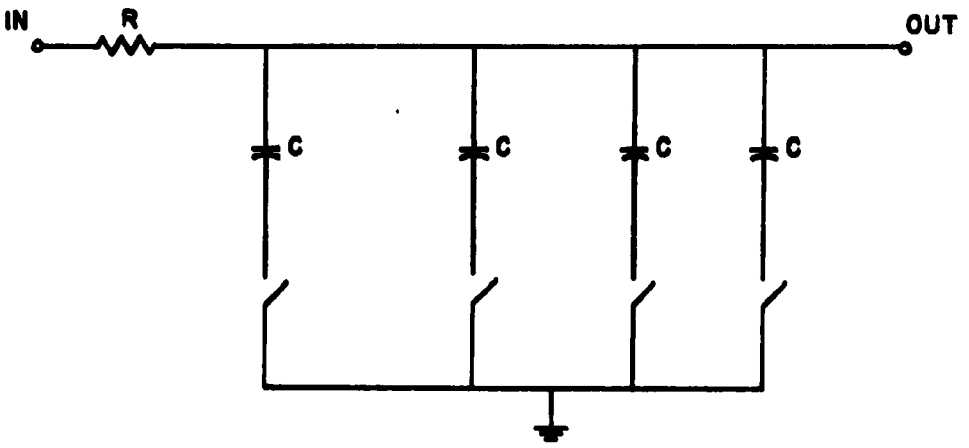


Figure 57 . Basic Digital Filter

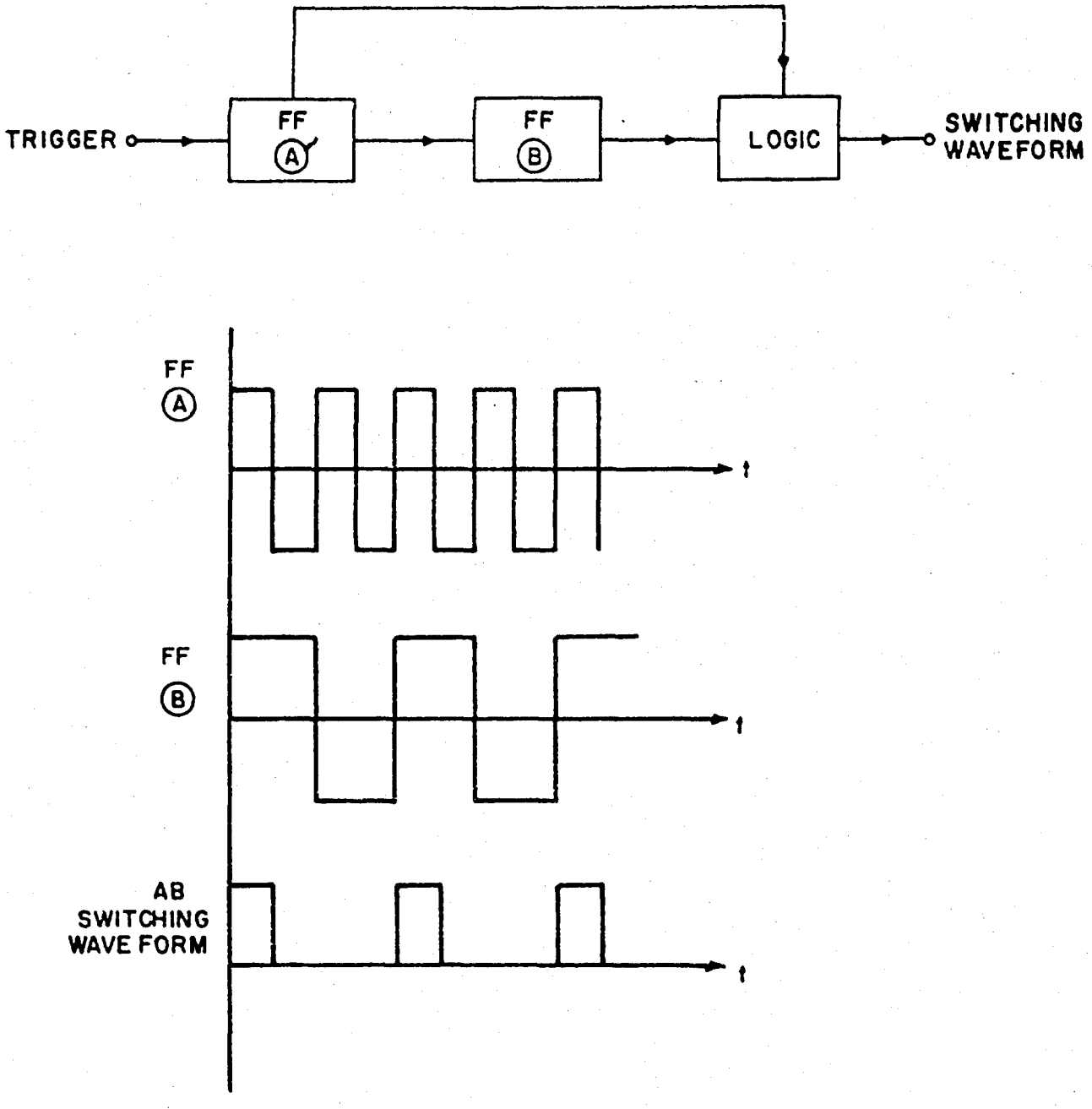


Figure 58. Low Frequency Switching Waveform Generation

eliminates the logic network and alleviates the problem of delay in the flip-flops. A four-stage shift register, for example, directly provides four waveforms similar to AB and spaced at the desired 90° intervals for sequentially operating the four switches. It is well to note here that the digital filter can be operated with three or more switched capacitors. The original choice of four was made because two flip-flops provided a convenient means for generating a switching waveform with a one-quarter duty cycle. However, the voltage transmission ratio T depends on N, the number of switched capacitors. More explicitly,

$$T = \frac{V_{out}}{V_{in}}$$

$$= \left[\frac{N \sin \pi/N}{\pi} \right]^2 .$$

The transmission ratio is 0.69 for N = 3 and is 0.81 for N = 4.

For rather arbitrary reasons, it was decided to use a four-stage shift register to generate the switching waveforms. The basic flip-flop used in the shift register and the trigger generator are shown in Figure 59. The interconnection of the four flip-flops and the added circuitry which insures that the shift register provides the desired one-quarter duty cycle is shown in Figure 60. The digital filter exclusive of the switch driving circuitry is shown in Figure 61. The emitter follower incorporating an attenuator was added to avoid loading the digital filter output at high frequencies. The output signal level in the data which follows is referred to the base and does not represent the attenuated output signal.

Two aspects of this digital filter were investigated. One point of concern was the switching noise which is primarily caused by transistor switching transients and differences in transistor leakage currents. As was mentioned in the Third Quarterly Report, simple compensating networks can be attached to

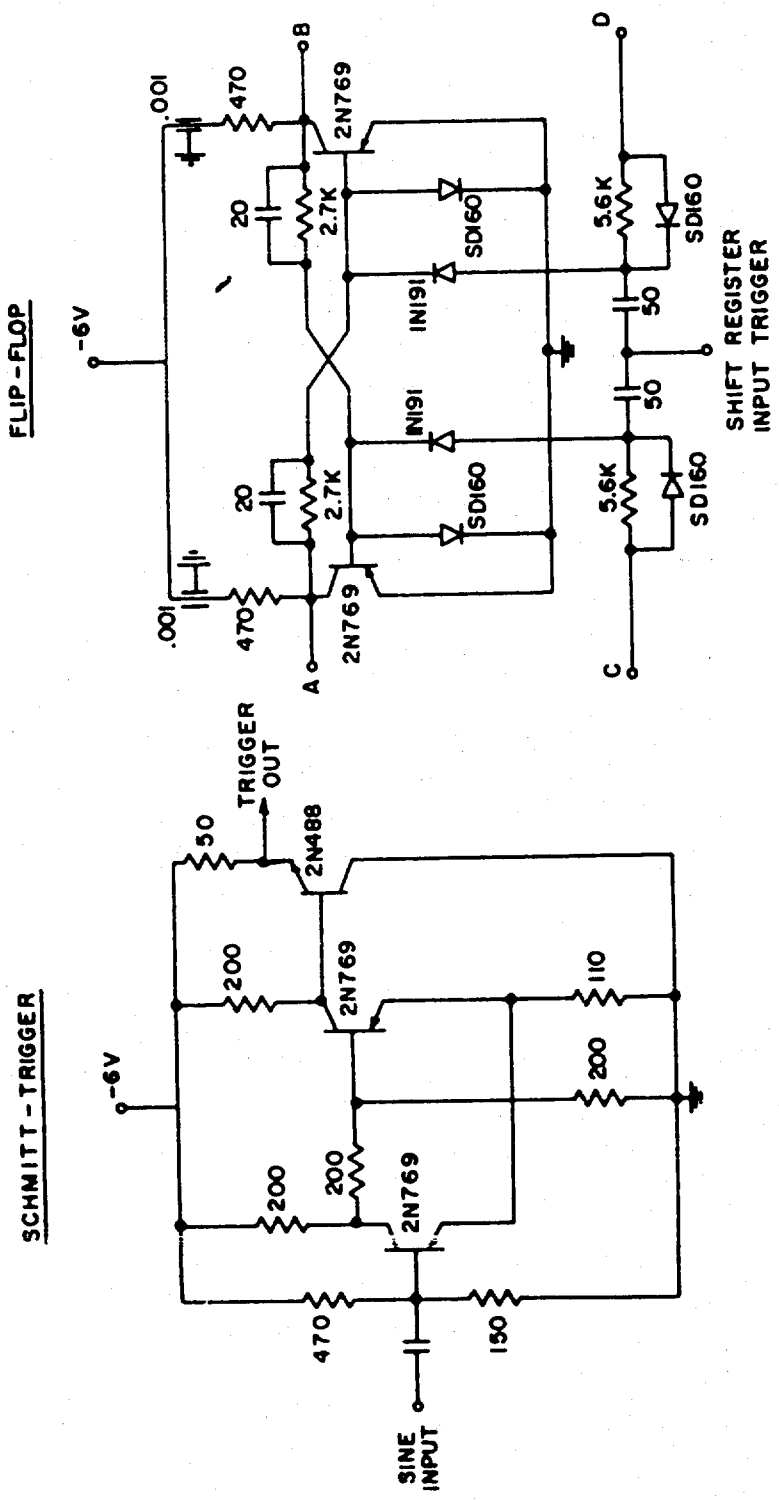


Figure 59. Basic Waveform Generating Circuits

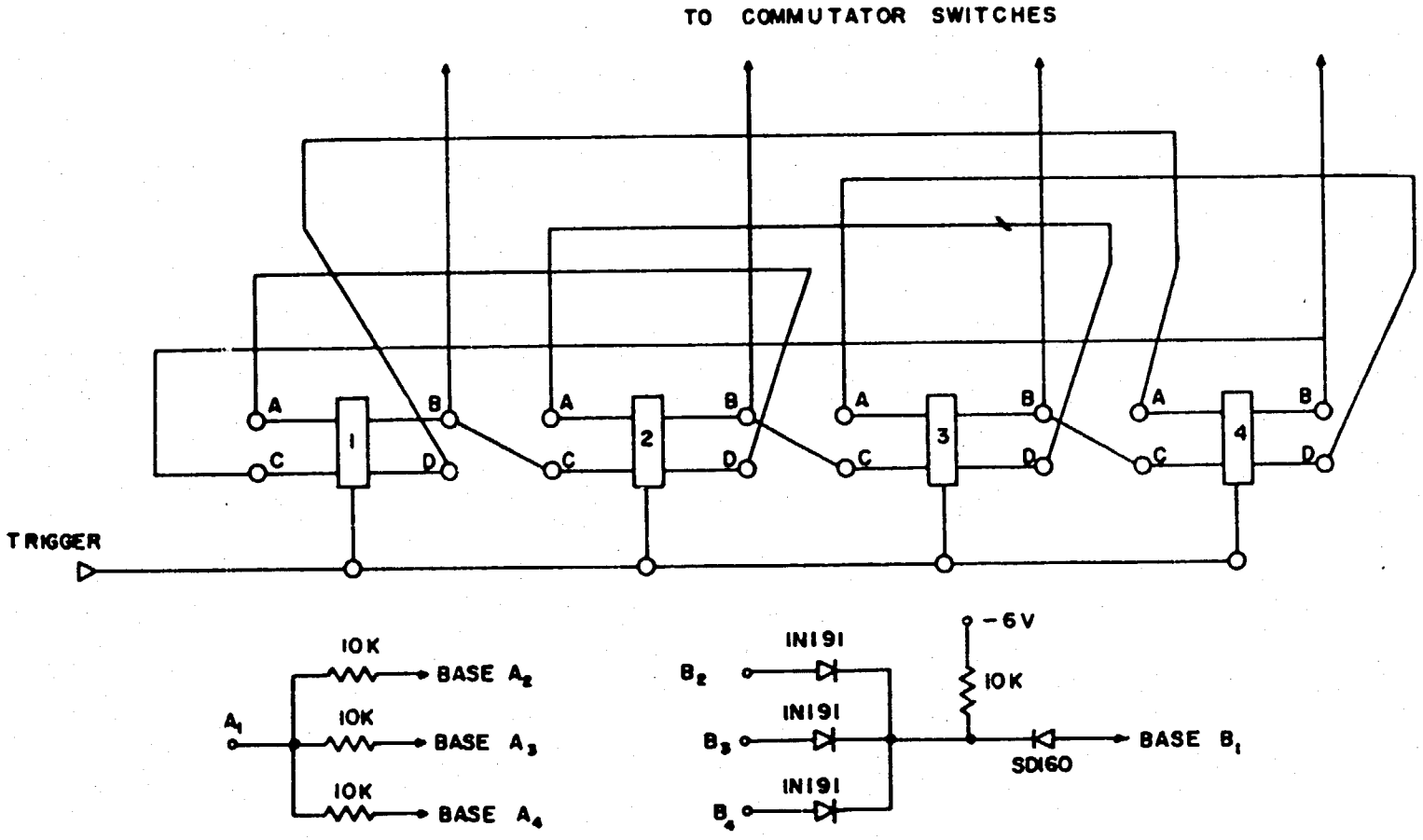


Figure 60 . Shift Register Connection Diagram

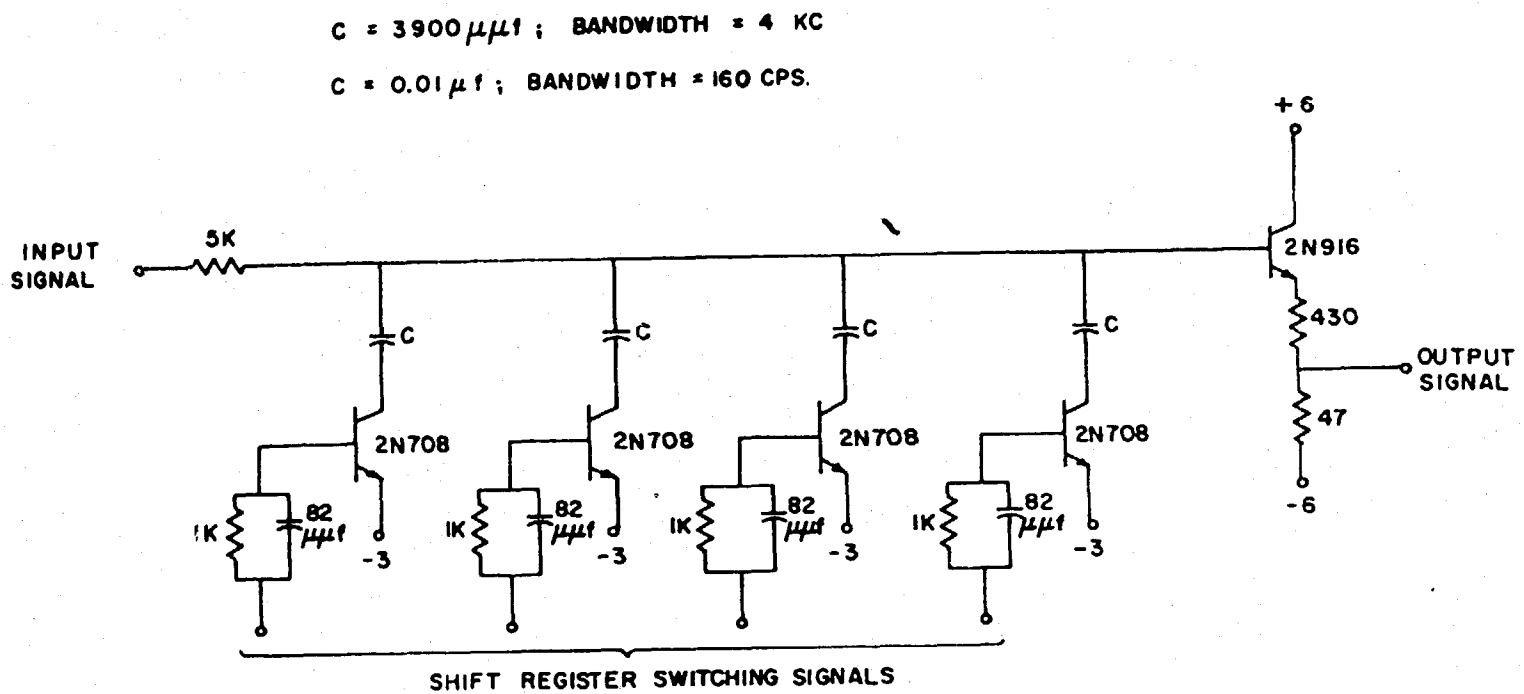


Figure 61. Digital Filter Circuit

each of the four capacitors to balance out the component of the switching noise at the commutating frequency. One of these networks is shown in Figure 62. Using these networks, the fundamental component of the switching noise could be reduced to less than 30 μv at frequencies up to 2 megacycles. If the compensating networks are removed, the fundamental component of the switching noise varied with frequency as shown in Figure 63 (for the random selection of components used in this circuit).

A second area of investigation was to determine how the digital filter transfer function depended on the commutating frequency. (If the switches were perfect, there would be no dependance.) The voltage transfer ratio is shown for commutating frequencies of 200 kc and 1 mc in Figures 64 and 65, respectively. Recall that the voltage transfer ratio for a four section digital filter should ideally be 0.81 at the center frequency. The measured values at several center frequencies are shown in Figure 66. Two significant points illustrated by these curves are that (1) the insertion loss of the filter increased with increasing center frequency, and (2) the bandwidth of the filter also increased with increasing center frequency. It is interesting to note that the measured points closely followed the theoretical asymptote at larger values of $| f - f_o |$. Sufficient time was not available to determine the cause of these phenomena. It might be postulated that both effects occurred because of an overlap in switching times primarily due to charge storage in the saturated transistor switches.

4. Conclusions

The digital filter provides a means of obtaining a band-pass filter which is amenable to micromin techniques. The digital filter also has the features that (1) the center frequency can be easily varied, (2) the bandwidth can be easily varied and (3) extremely narrow bandwidths (less than 1 cps) are achievable. The digital filters constructed have been operated at frequencies ranging from 100 cps to 2 mc.

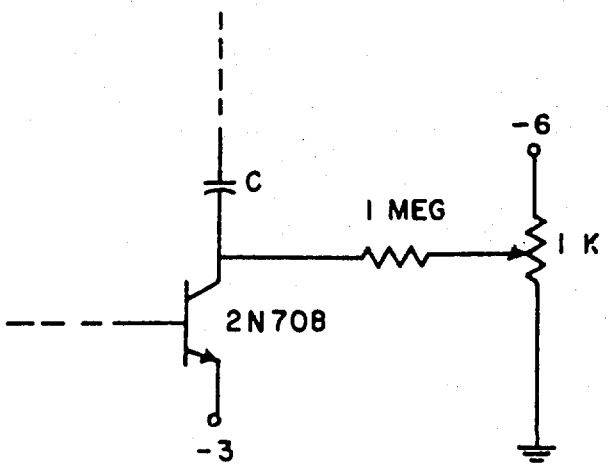


Figure 62 . Noise Balancing Network

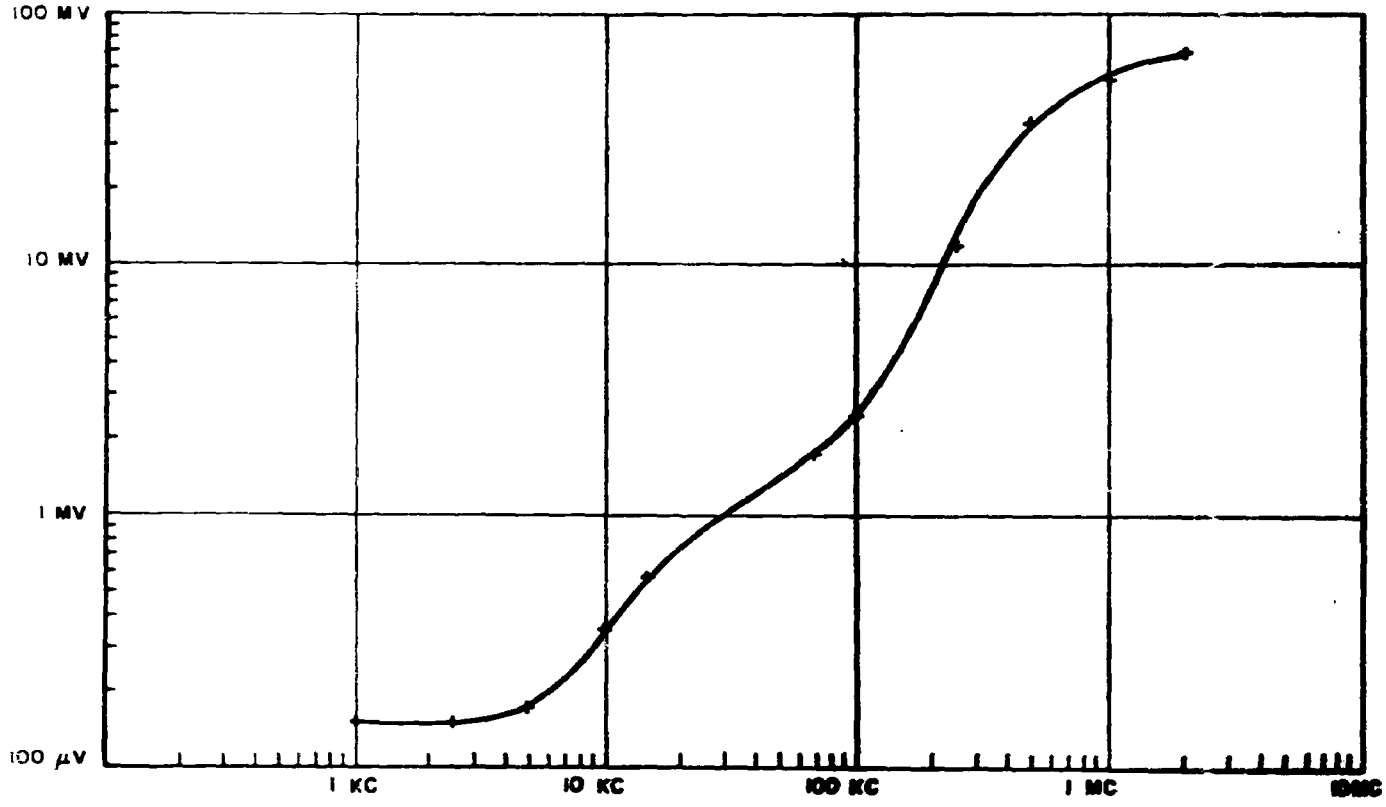


Figure 63. Fundamental Component of Commutating Noise as a Function of Center Frequency

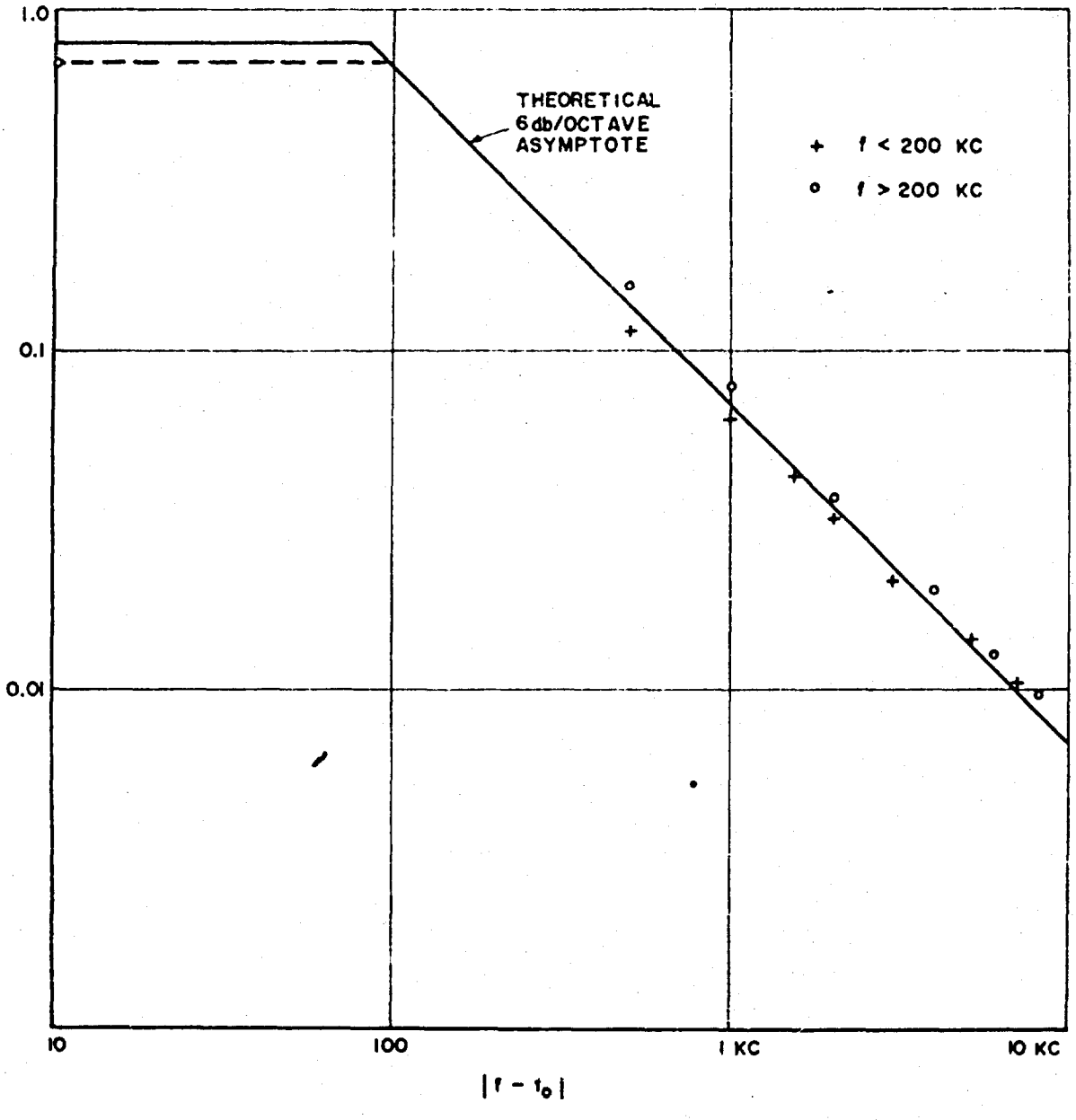


Figure 64. Digital Filter Voltage Transfer Ratio at 200 kc Center Frequency with 160 Cycle Theoretical Bandwidth

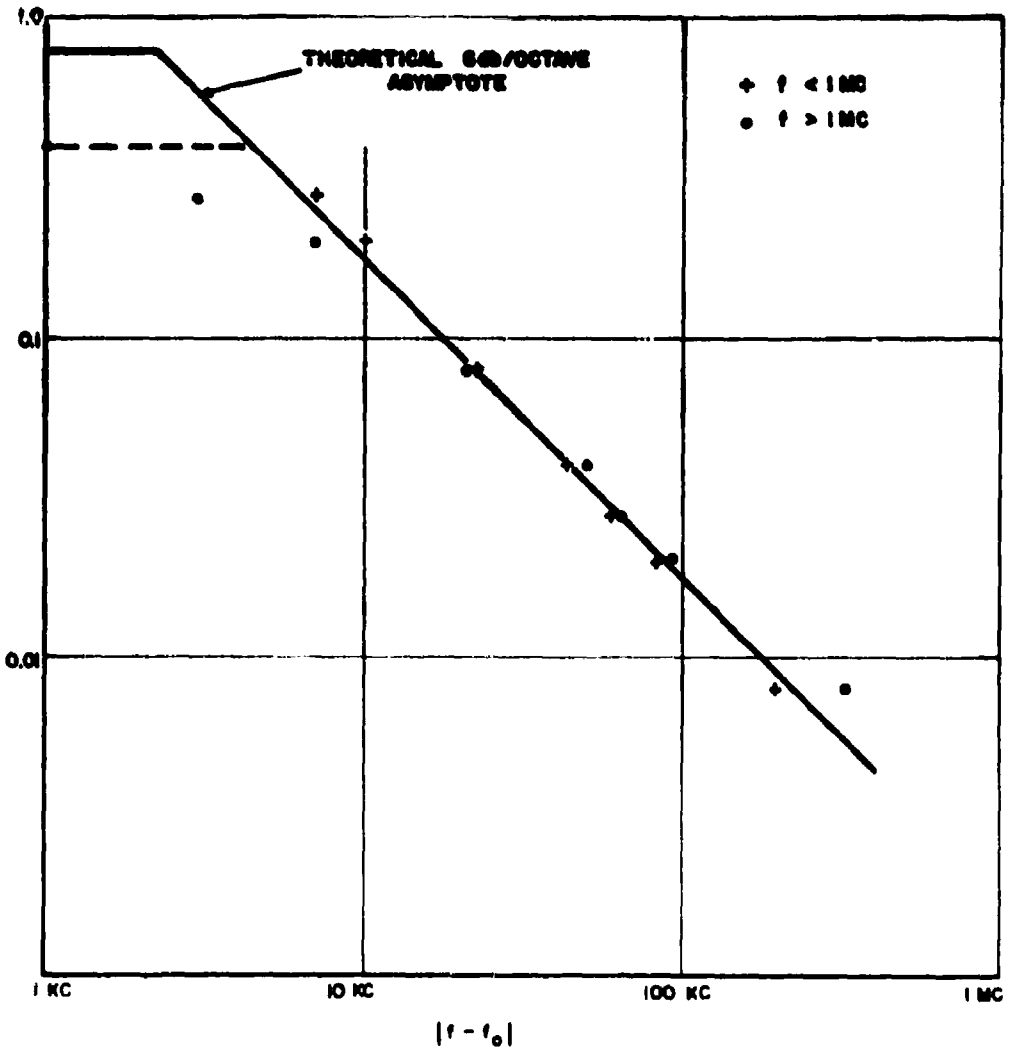


Figure 65. Digital Filter Voltage Transfer Ratio at 1 Mc Center Frequency with a 2 kc Theoretical Bandwidth

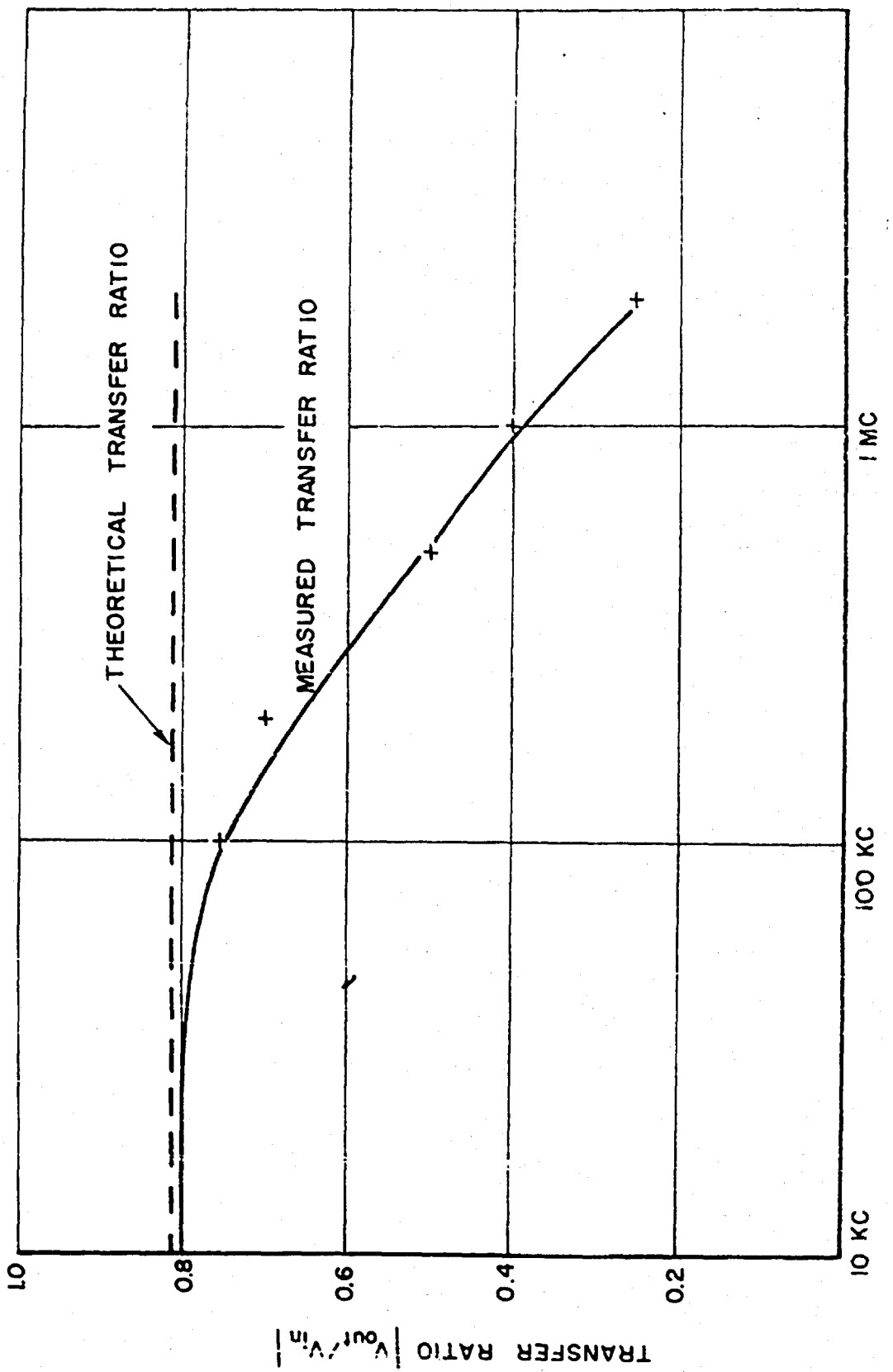


Figure 66. Voltage Transfer Ratio at Center Frequency as a Function of Center Frequency

V. IDENTIFICATION OF KEY TECHNICAL PERSONNEL

A. BIOGRAPHIES

P.W. Becker

Mr. Becker received his M.S.E.E. from the Technical University of Denmark in 1950.

He has been employed as an engineer by the General Electric Company since 1956, first with Industry Control at Roanoke, Virginia, later at the Glass Machine Operation in Cleveland, Ohio, and then at Philadelphia, Pennsylvania with the Development Laboratory of the Switch Gear Department. He joined Advanced Circuits component of the Electronics Laboratory in 1958. Since joining General Electric Company, he has worked with computers, dielectric materials, electromechanical devices, magnetic circuits, and semiconductor circuits.

Gordon H. Danielson

Mr. Danielson received his B.S. degree in electrical engineering from Michigan State University in 1957. He is currently working toward the Ph.D. degree at Syracuse University.

After graduation from college, Mr. Danielson joined the General Electric Company as a participant in the Honors Program. Upon completion of this program he became a member of Advanced Circuits component of the Electronics Laboratory. He has had experience in the fields of communication, data presentation, electromechanical devices, semiconductor circuits, radar, and vacuum tubes.

Mr. Danielson is a member of the IRE.

C. DeGarmo

Mr. DeGarmo received his B.S.E.E. from Syracuse University in 1932. He was an instructor at Syracuse University from 1932-33, and then taught high school mathematics from 1933-42. In 1942, he received an M.S. in

Public School Administration from Syracuse University. During the war years, Mr. DeGarmo taught courses in Analytical Geometry to members of the Army Specialized Training Program.

In 1942, Mr. DeGarmo joined General Electric as a Design Engineer in the Apparatus Department, and for the first two years worked on the design generator components of Navy Destroyer Escort turbines. In 1944 he became concerned with jet engine design, designing frame, assembly, weight reduction, etc.

From 1945 to 1957, he carried out mechanical design work on General Electric's carrier current rack and panel equipment line. Part of this time, all aspects of this line's mechanical design, development, and cost reduction were his sole responsibility.

Louis J. Ragonese

Mr. Ragonese received his B.E.E. and M.E.E. degrees from Syracuse University in 1956 and 1958, respectively.

During the summer of 1956, he was an engineer with the Color Television Advanced Circuit Development Group of the General Electric Company. He returned to Syracuse University as a Graduate Research Assistant with the Electric Engineering Department until June 1958. The research work involved the analysis, processing and display of certain developmental radar signals.

From July 1958, Lieutenant Ragonese served three years with the U.S. Air Force in the specialty category of electronics engineer. During his full tour of duty, he was involved in the study and design of high speed transistorized digital computer subsystems. The work included the design of circuits and their logical interconnection.

Mr. Ragonese is a member of Eta Kappa Nu, Pi Mu Epsilon, Tau Beta Pi, and the Institute of Radio Engineers. He joined the Advanced Circuits and Integrated Electronics Group upon release from active duty in July 1961.

Best Available Copy

Robert E. Warr

Mr. Warr received his B.A. degree in physics from Fisk University in 1949 and his M.S. degree in physics from Purdue University in 1951. He became a member of Sigma Pi Sigma, Honorary Physics Society, while pursuing his studies at Purdue.

From 1951 to 1953, he was employed as a physicist at the National Bureau of Standards. From 1953 to 1956, he was employed as a physicist at the Diamond Ordnance Fuze Laboratories.

In 1956, he joined General Electric as a member of the Light Military Electronics Department. While there he participated in a series of engineering assignments and worked as Project Engineer in programs of research and development in reliability, microminiaturization, nuclear radiations effects and optical lasers.

He is the author or co-author of the following articles: "Structure of Oxide Scales on Nickel Chromium Steels", Corrosion, November 1956; "An Approximate Method of Forming a Confidence Interval on Predicted System Reliability", IRE Transactions on Reliability and Quality Control, June 1959; "Design Techniques for Reliability", Seventh National Symposium on Reliability and Quality Control, January 1961; "Seismic Switch", Diamond Ordnance Fuze Publication, 1954 and the following internal General Electric papers: "Reliability of Modular Assemblies", "Incipient Failure Detection", "Circuit Classification and Evaluation", "Part Rejection Analysis", "Collection, Analysis and Reporting of Reliability Test Data", and "Pulsed Ruby Optical Laser".

John A. A. Raper (Consultant)

Mr. Raper studied engineering at the University of London in 1948-50. He completed his undergraduate work at Pratt Institute and received his B.E.E. degree with honors in 1952. Since coming with General Electric, he has completed the Company technical course in Switching Circuit Analysis.

Mr. Raper was employed by the Post Office Telephone Department in England where he was concerned with multichannel telephone and telegraphy equipment. He served as a First Lieutenant of the 19th Air Formation Signals Unit in Rangoon and Singapore in charge of similar equipment.

Mr. Raper joined General Electric in 1952 as a member of the Engineering Program, a one-year series of assignments in different engineering functions of the Company. In 1953, he became a member of Advanced Circuits of the Electronics Laboratory. His initial work was design and development of transistor circuitry for use in communications type equipment. Mr. Raper received the General Electric Managerial Award given for "outstanding contribution to development of transistor radio circuitry and the evaluation and application of new semiconductor devices."

From 1956 until 1960, he has been Project Engineer for a number of development projects in the area of miniaturized communications equipment with emphasis being placed on the use of novel device and circuitry techniques.

In July 1960, Mr. Raper was appointed Program Manager - Microelectronics for the Electronics Laboratory in which position he was responsible for integrating the activities of the Electronics Laboratory in this field. In July 1961, he was appointed Manager - Advanced Circuits and Integrated Electronics.

Mr. Raper is a member of Tau Beta Pi and IRE and is the holder of four patents. Mr. Raper is a co-author of "Transistor Circuit Engineering," John Wiley and Sons, Inc., 1957, and has given or published the following articles and papers: "Transistorized Broadcast Receivers, "IRE National Convention, 1954; "A Low Level Diode Limiter," IRE Circuit Theory Transactions, March 1956; "Transistorized Broadcast Receiver Design," IRE Chicago Meeting, October 1955; "A Transistorized Digital to Analog Converter," Electronics, December 1957; "A Transistorized Broadcast Receiver," Electrical Engineering, December 1954.

J.J. Suran (Consultant)

Mr. Suran studied at Queen's College prior to attending Columbia University where he received a B.S.E.E. in 1949. He did graduate work in Electrical Engineering at Columbia in 1949-1950, and in 1951-1952 studied graduate physics at Illinois Institute of Technology.

Mr. Suran joined the J.W. Meaker Company in 1949 as a development engineer. Until 1951, he was engaged in research and development work in servo-mechanism control systems. This consisted of circuit and system developments centered about such designs as electronic sensing devices and circuits to measure air flow, servo-systems to effect automatic control of porosity in paper and sheet plastic manufacturing processes, thyratron control circuits for high-voltage spark-gap machinery, etc.

In 1951, he joined Motorola, Inc., and until 1952 he was concerned with research and development in mobile communication systems. This work consisted of problems in impulse noise and narrow band FM receivers, distortion of FM signals by linear networks, information theory analysis of FM communication systems, orthogonal multiplexing, transient analysis of lumped stagger-tuned filters and non-linear amplifiers. During this period such circuits as standard amplifiers, non-linear pre-amplifiers, sampling circuits for FM receivers, super-regenerative amplifiers, active filters, peizoelectric oscillators, noise-suppression limiters and distributed filters were developed.

Mr. Suran joined the General Electric Electronics Laboratory in 1952. Since then he has been concerned with research and development in the application of solid state components to advanced circuits. This has consisted of investigation of such problems as transient response of transistor amplifiers; solution of the diffusion equation for transistors; electric field effects in transistor tetrodes and double-base diodes; negative-resistance circuits, high-power and high-temperature operation of various semiconductor devices; and the design of novel ferrite components such as the transfluxor for pulse-circuit applications. During this period he

was involved in the development of detectors using novel semiconductor devices; astable, monostable, and bistable switching circuits employing transistors and double-base diodes; measuring equipment for the double-base diode; regenerative pulse amplifiers; digital-to-analog converters, high-speed switching networks, binary and decimal counters, and the like.

In 1954 he became a Project Engineer and in 1956 he was made Consulting Engineer - Solid State Circuits. In 1955, he was given the General Electric Managerial Award for his contributions to advances in the art of solid state circuits.

Mr. Suran was made Manager - Advanced Circuits in 1957, and since then has directed the research and development efforts of 27 engineers and eight technical and administrative personnel in this field.

In July 1961, Mr. Suran was appointed Manager - Electronics Devices and Applications Laboratory. During a reorganization in October 1961 he was appointed Manager - Electronic Applications Laboratory. This Laboratory consists of professional and technical personnel working in instrumentation, electronic devices, solid state materials and microelectronics.

He is a Licensed Professional Engineer in the State of New York, a Member of RESA, an Associate Member of the AIEE, and that organization's Electronic Circuits Committee. He is also a Senior Member of the IRE, a Member of the IRE Circuits Committee, and Chairman of the Solid State Circuits Sub-Committee.

Mr. Suran is the holder of eight patents and twenty patent applications on control systems and solid state circuits. He is the co-author of two books: Principles of Transistor Circuits, John Wiley and Sons, 1953, and Transistor Circuits Engineering, John Wiley and Sons, 1957. He is also the author or co-author of the following articles and publications: "Electric Control of Porosity," Modern Plastics, February 1951; "Effect of Weak Betas on the Breakdown of Dielectric Gaps," Nucleonics, June 1951; "Electric Control of Air-Flow Porosity in Dielectric Sheet Materials," Transactions of the ASME, January 1952; "Transient Analysis of Junction

Transistor Amplifiers," Proc. of IRE, September 1953; "Transistor Transient Response," Tele-Tech, November 1953; "Transient Response of the Grounded-Base Transistor Amplifier with Small Load Impedance," Journal of Applied Physics, November 1953; "Transient Response of Selective Networks and Impulse Noise in Narrow-Band F.M. Receivers," 1954 Convention Record of the IRE, March 1954; "Relay Properties of the Double-Base Diode," Airborne Electronics Digest, May 1954; "Steady State Solution of the Two-Dimensional Diffusion Equation for Transistors," Journal of Applied Physics, July 1954; "Effect of a Transverse Electric Field on Carrier Diffusion in the Base Region of a Transistor," Journal of Applied Physics, August 1954; "Double-Base Expands Diode Applications," Electronics, March 1955; "Low-Frequency Circuit Theory of the Double-Base Diode," IRE Transactions ED, April 1955; "Semiconductor Diode Multivibrators," Proc. of IRE, July 1955; "Transistors General Multiwaveforms," Electronics, July 1955; "Impulse Noise in Narrow-Band F.M. Receivers," Communications and Electronics, AIEE, September 1955; "Two Terminal Analysis of Transistor Multivibrators," Trans. of PGCT, Vol. CT-3, March 1956; "Circuit Properties of the PNPN Transistor," Proc. of National Conference on Aeronautical Electronics, May 1956; "Small-Signal Wave Effects in the Double-Band Diode," Trans. of PGED, Vol. ED-4, January 1957; "Design of Junction Transistor Flip-Flops by Driving Point Impedance Methods," 1957 IRE National Convention Record, March 1957; "Temperature Characteristics of the Transfluxor," IRE Trans. PGED, April 1957; "Multihole Ferrite Core Configurations and Applications," Proc. of IRE, August 1957; "Transient Response Characteristics of Uni-junction Transistors," Trans. of PGCT, Vol. CT-4, No. 3, September 1957; "Gamma-Ray Monitor has High Reliability," Electronics, November 1957; "Digital Analogue Converter Provides Storage," Electronics, December 1957; and "Transistor Monostable Multivibrators for Pulse Generation," Proc. of IRE, June 1958.

B. APPROXIMATE ENGINEERING MAN HOURS

Fourth Quarter

	Contact	Company Programs	Consulting
R.E. Warr	68	348	—
L. Ragonese	172	185	—
G.H. Danielson	208	120	—
G. Jansen	40	—	—
P.W. Becker	191	—	—
C. DeGarmo	102	—	—
J.J. Suran	—	—	40
Additional Professional Personnel	110	344	—
	891	997	40

Total 1928 Man Hours.

Totals (1st Year)

1st Quarter	1114 Man Hours
2nd Quarter	1796 Man Hours
3rd Quarter	1791 Man Hours
4th Quarter	1928 Man Hours
Total	6629 Man Hours

APPENDIX B-1

Long Term Versus Short Term Reliability of Circuits and Systems.

(a) Introduction.

Relability of Systems and Circuits depends upon such factors as component distributions, cooling arrangements and design tolerances. In the following a new approach to the design of reliable circuits and systems will be described. The new approach shows how circuit reliability may be optimized in terms of the above factors, and shows when it is necessary to resort to redundancy.

Systems and circuits fail due to drift or catastrophic failure of the components; the word component is here used in its widest sense. If circuits are worst-case designed for large component tolerances, protection is obtained against failures due to component drift. Design for large component tolerances unfortunately leads to low resistor values and high circuit temperature. The catstrophic failure rate of components per 1000 hours, λ_c, increases with circuit temperature. It is thus seen that the most reliable circuit is the circuit which is designed so that P(S) has been maximized. P(S) is the joint probability of the circuit not failing due to drift of components and not having catastrophic component failures.

It should be realized that P(S) is time dependent. The term "most reliable circuit" is meaningful only when it has been specified at which time or over which time interval the circuit should be reliable.

On the next pages the following problem will be solved: how is P(S) maximized?

(b) Component Distributions.

It is assumed that all probability distribution curves are known for all circuit component parameters as functions of time and temperature. To simplify the following description let it be assumed that all distributions are truncated.

(c) Worst-Case Design of N Circuits.

Due to our knowledge of the component distributions we can worst-case design circuits which at any specified time or time interval has P(D) = 1 for the temperature ranges T_o to T_1, T_o to T_2,... and T_o to T_{N-1}. $T_o < T_1 < T_2 < \ldots < T_{N-}$ P(D) is the probability that a circuit does not fail due to drift of components at the specified time. Let it also be assumed that we have designed a circuit which has P(D) = 1 for just the reference temperature T_o. All N circuits use the same cooling arrangement, power supplies and types of components; all N circuits are designed so that they can drive the same load.

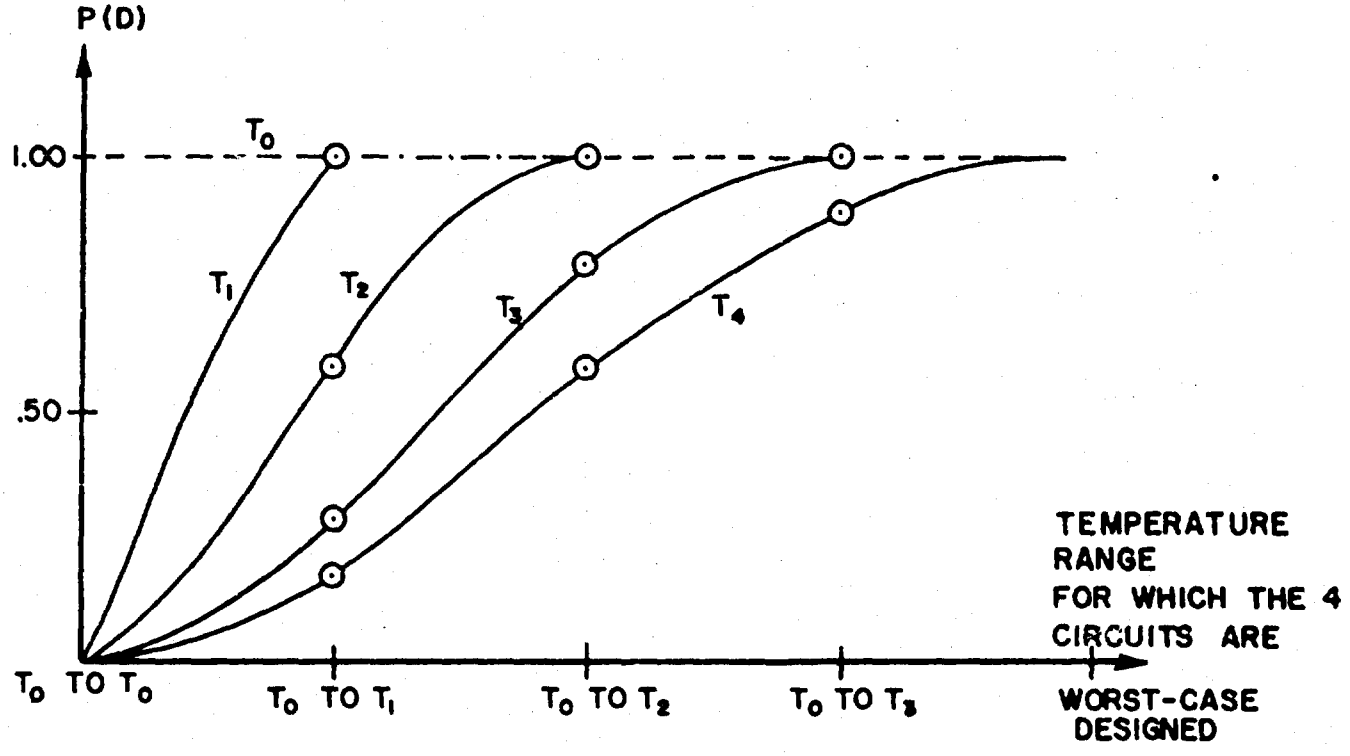
Notice that if the distributions have "tails", we do not obtain P(D) = 1 for any circuit. This is why the assumption of truncated distributions simplifies the description.

The total number of designed circuits is N. To facilitate the following description let it be assumed that 100 copies are built of the "T_o to T_1" -circuit, 100 copies are built of the "T_o to T_2" -circuit, etc. The total number of circuits built is 100 N.

(d) P(D) as a Function of Temperature.

If the temperature of all 100 N circuits are maintained at T_o obviously none of the circuits would fail due to component drift. If the temperature is raised to T_1 some of the 100 circuits which were designed to operate at T_o will fail. None of the remaining 100 (N-1) circuits will fail due to component drift. If the temperature of all 100 N circuits is raised to T_2, most of the first 100 circuits will fail, some of the next 100 circuits will fail, and none of the last 100 (N-2) circuits will fail due to component drift, etc.

Let T_x be a general expression for T_o, T_1,..., and T_{N-1}. The worst-case design temperature range is then T_o to T_x. Figure 1 shows P(D) versus "T_o to T_x". Such S-shaped curves have been obtained by computer simulation as described in paragraph (e).



P(D), THE PROBABILITY THAT A CIRCUIT DOES NOT FAIL DUE TO DRIFT OF COMPONENTS. THE CURVES SHOWN WERE OBTAINED BY ACTUAL COMPUTER SIMULATION OF CIRCUIT FAILURE.

FIGURE 1

(e) Computer-Simulation of Circuit Failure.

The question of whether a circuit will work with a certain set of true component values may be decided by substituting the true component values in some set of inequalities. It is assumed that if and only if all inequalities are satisfied, the circuit will work with the set of true values in question. We write down the N sets of inequalities corresponding to the N circuits.

(1) We choose at random true values of the components corresponding to T_o distributions, and substitute these values into the N circuits. This is repeated a large number of times and it is seen that all N sets of inequalities always are satisfied. The reason being that all N circuit designs were determined so that they would work satisfactorily at temperature T_o.

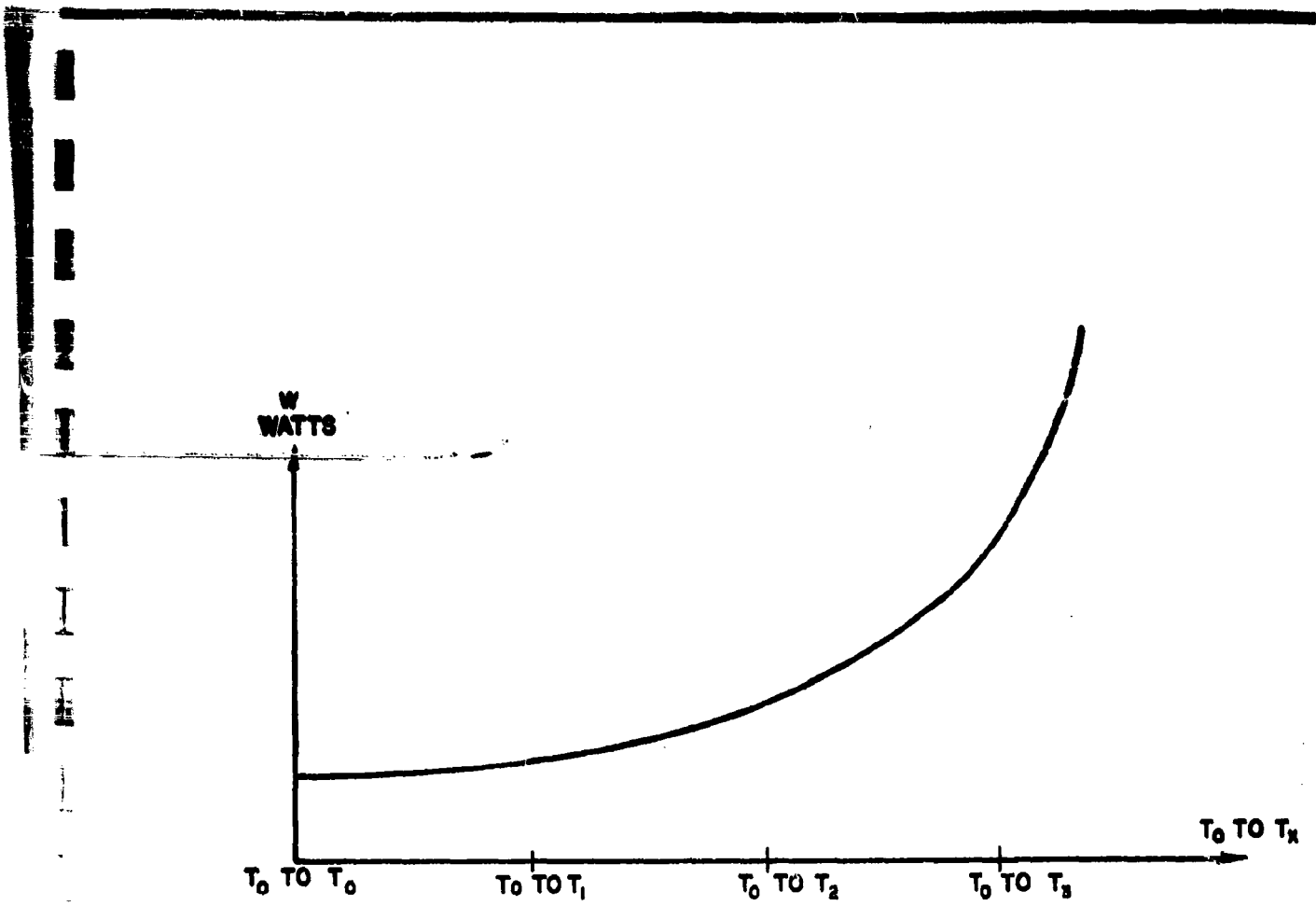
We draw the horizontal line through P(D) = 1 on Figure 1, and mark the line T_o.

(2) We choose at random true values of the components corresponding to the T_1-distributions, and substitute these values into the N sets of inequalities. It is seen that the N-1 circuits designed for the temperature ranges T_o to T_1, T_o to T_2, etc. all hold up. The first circuit, which was designed to work only at T_o will fail in many instances, it has a P(D) which is less than one. We draw the curve T_1 on Figure 1.

(3) The simulation is repeated using true component values corresponding to the T_2-distribution, T_3-distribution, etc. We draw the curves T_2, T_3, etc. on Figure 1.

(f) Power Dissipation, W, versus "T_o to T_x"

Next the power dissipation, W_o, W_1, etc. to W_{N-1}, of each of the N circuits is computed. It will be found that W increases very rapidly, almost exponentially, with "T_o to T_x". Figure 2 shows W as a function of "T_o to T_x".



POWER DISSIPATION W AS A FUNCTION OF "T_0 TO T_X", THE TEMPERATURE RANGE FOR WHICH A CIRCUIT IS WORST-CASE DESIGNED.

FIGURE 2

(g) The Operating Temperature of a Circuit, T_{op}.

For a given cooling arrangement each of the N circuits will arrive at some temperature - equilibrium when the circuit has been operating for some time.

To avoid discussions of circuit, worst-case, surface, skin, maximum, ambient, and hottest-point temperature, let this temperature be called the operating temperature. A definition of T_{op} will depend upon the circumstances, and is immaterial for the following description. T_{op} may be computed by some expression similar to:

$$T_{op} = W \times \text{Constant} + T_o \qquad (1)$$

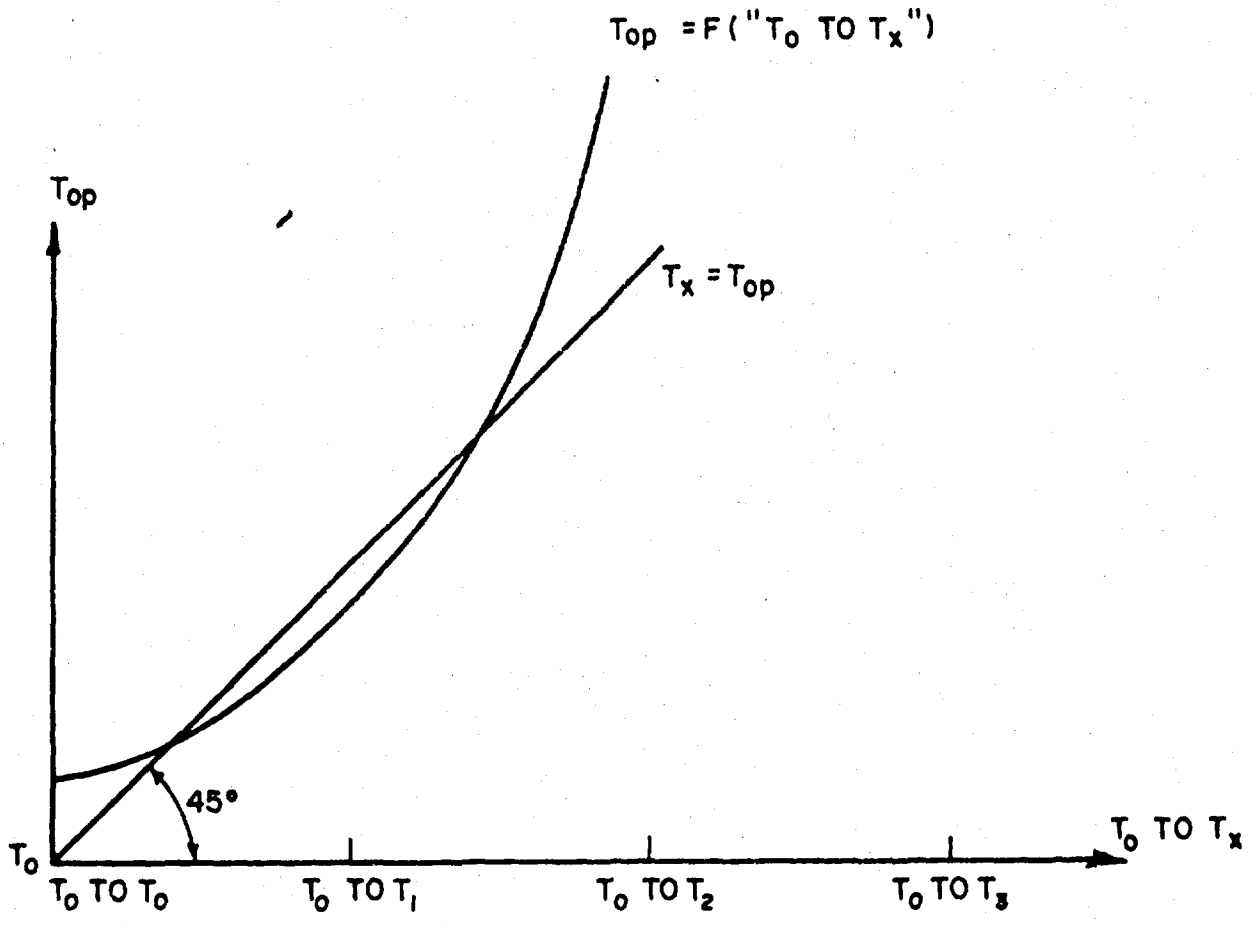
where the constant will descrease with better cooling arrangements and lower packing densities.

Equation (1) states that T_{op} is a function of W, and consequently also a function of "T_o to T_x", see Figure 2. T_{op} as a function of "T_o to T_x" is shown on Figure 3. This curve is very important as it links the maximum temperature T_x for which a circuit was worst-case designed to the natural temperature of the circuit. The curve will be used twice: first to find P(D) as a function of "T_o to T_x", see paragraph (i), and secondly to find the catastrophic failure rate, see paragraph (j) and Figure 4. The curve is referred to as the $T_{op} = F(\text{"}T_o \text{ to } T_x\text{"})$ curve, and its location depends upon the constant from Equation 1.

(h) The 45° line, $T_x = T_{op}$.

Next the curve $T_x = T_{op}$ is added to Figure 3. The curve is helpful in so far that it facilitates the following description. When Equation 1 has the simple linear form which was assumed in the previous paragraph the curve becomes a 45° line.

Notice that a circuit which has been worst-case designed to work at reference temperature T_o only, always has a natural temperature which is higher than the reference temperature, See Equation 1. The reference temperature is often room temperature. Consequently, the $F(\text{"}T_o \text{ to } T_x\text{"})$ - curve will lie above the 45° line for $T_x = T_o$.



THE OPERATING TEMPERATURE T_{op} AS A FUNCTION OF "T_o TO T_x", THE TEMPERATURE RANGE FOR WHICH A CIRCUIT IS WORST-CASE DESIGNED.

FIGURE 3

Also notice that for sufficiently high values of T_x, the natural temperature of a circuit is higher than the maximum temperature for which the circuit was worst-case designed. Consequently the F("T_o to T_x") curve will lie above the 45^o line for high values of T_x.

The 45^o line may or may not intersect the F("T_o to T_x") curve depending on the value of the Constant in Equation 1. The Constant depends upon cooling arrangements, packing densities, etc. as stated in paragraph (g).

(i) The F curve and the 45^o line, Three Possibilities.

Figure 4 illustrates the three possible locations of the F("T_o to T_x") curve with respect to the 45^o line. If T_{op} of a circuit falls in the temperature range for which the circuit was designed, P(D) is 1.0 for the circuit. If T_{op} of a circuit is above the temperature-range for which the circuit was designed, P(D) may be less than 1.0. The actual value of P(D) may be found by interpolation between the T-curves of Figure 1. In this way the three figures in the lower half of Figure 4 were obtained.

From the curves of Figure 4 we can now answer the questions of how P(D) for a circuit depends upon:

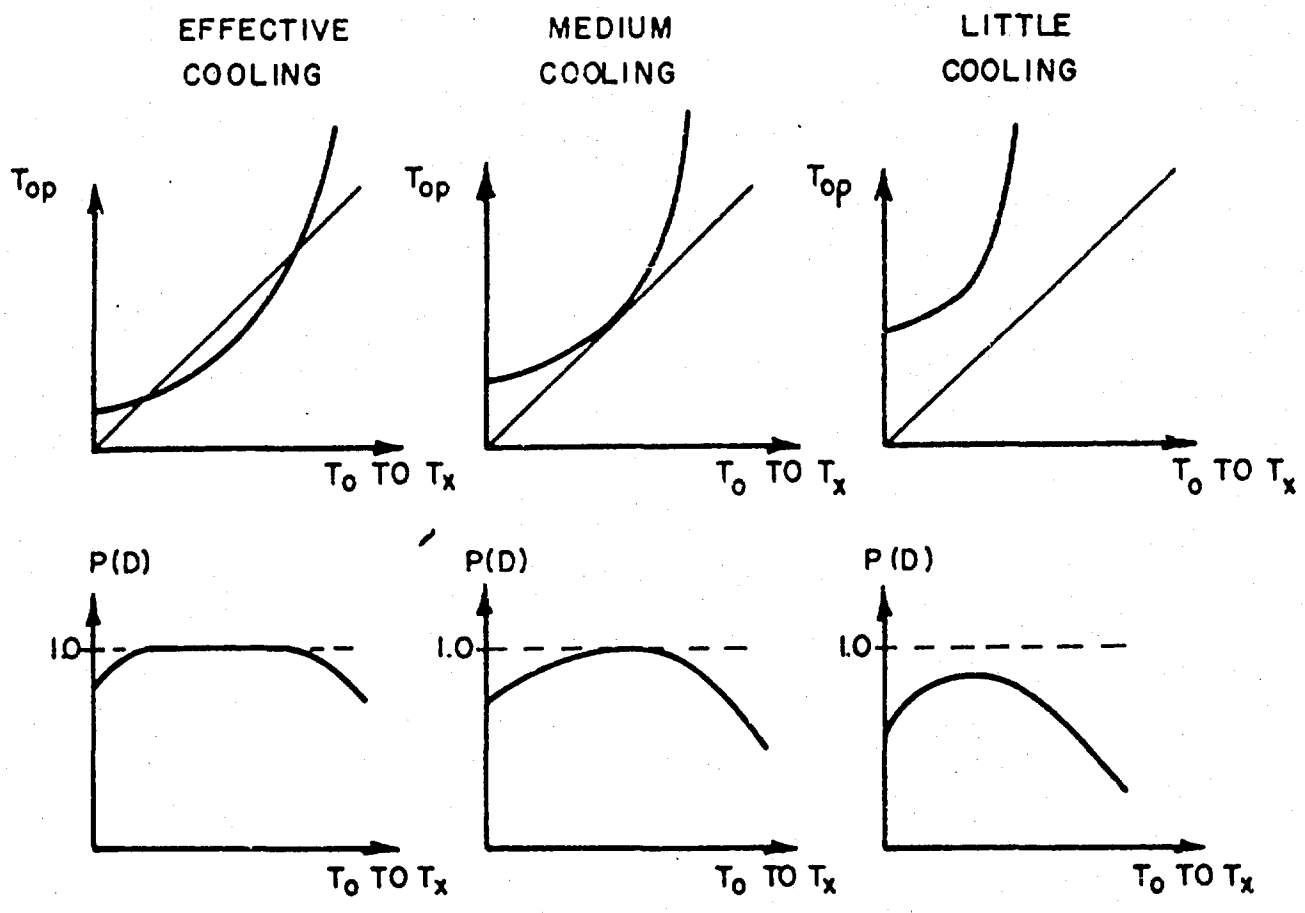
(1) the temperature range for which the circuit was worst-case designed

(2) the cooling arrangement

(j) The Catastrophic Failure Rate

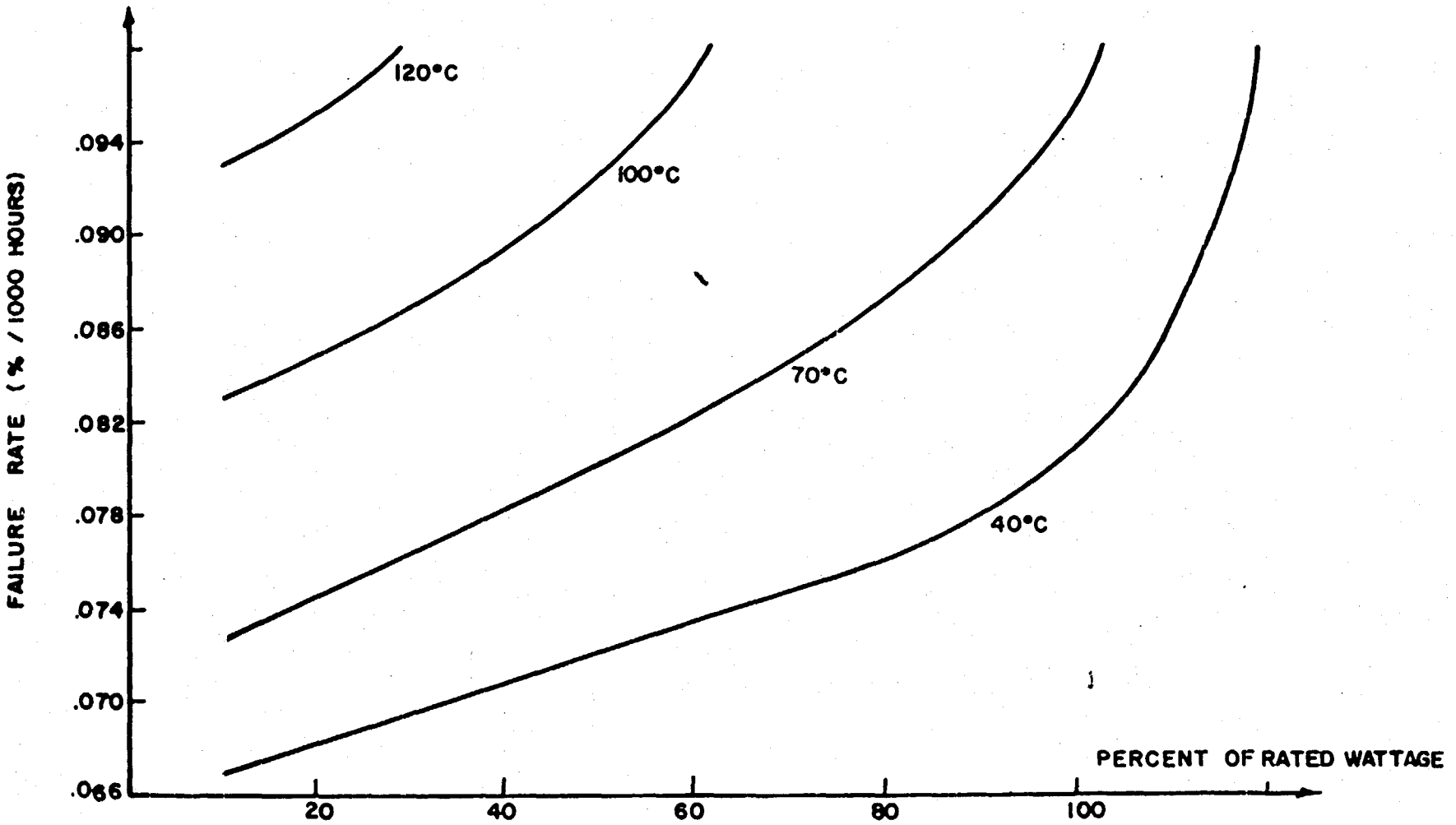
Information is available in the literature indicating the catastrophic failure rate per 1000 hours of the components as a function of temperature and $\frac{\text{actual power dissipation}}{\text{rated power dissipation}}$. Figure 5 shows how such curves may look for composition resistors. From such information, λ, the catastrophic failure rate per 1000 hours for each circuit can be computed.

Notice that with increasing T_x values the following factors will increase: W, T_{op} and λ.



INFLUENCE OF THE COOLING ARRANGEMENTS UPON P(D). THE VALUE OF THE CONSTANT IN EQUATION I WILL DECREASE WITH IMPROVED COOLING OF THE N CIRCUITS.

FIGURE 4



FAILURE RATES FOR VARIABLE COMPOSITION RESISTORS. RESISTANCE VALUES BELOW 50K

FIGURE 5

(k) Success-Probability P(S) of a Circuit as a Function of Time.

As stated is paragraph (c) the probability at some specified time of a circuit not having failed due to drift of its components is called P(D). The probability of a circuit not having failed due to catastrophic component failures at time t is $e^{-\lambda t}$. The probability that the circuit still works at the specified time is consequently:

$$P(S) = P(D)\, e^{-\lambda t}$$

Figure 6 shows P(S)-curves for 4 circuits designed with different "T_o to T_x" -values. Notice that the "T_o to T_3"-curve and the "T_o to T_o"-curve intersect at about 70,000 hours. Moreover, the curve with the smallest λ -value, the "T_o to T_o"-curve, intersects all curves which have a higher P(S)-value at t=0. This indicates the importance of time in reliability considerations.

(l) Success-Probability $P_s(S)$ of a System as a Function of Time

From the curves of Figure 6 it is possible to compute the success-probability $P_s(S)$ of systems built of circuits, each system using circuits designed with the same "T_o to T_x"-value. Figure 7 shows two such $P_s(S)$-curves. Notice that the average of $P_s(S)$ over any interesting time-interval may be found from Figure 7 by integration.

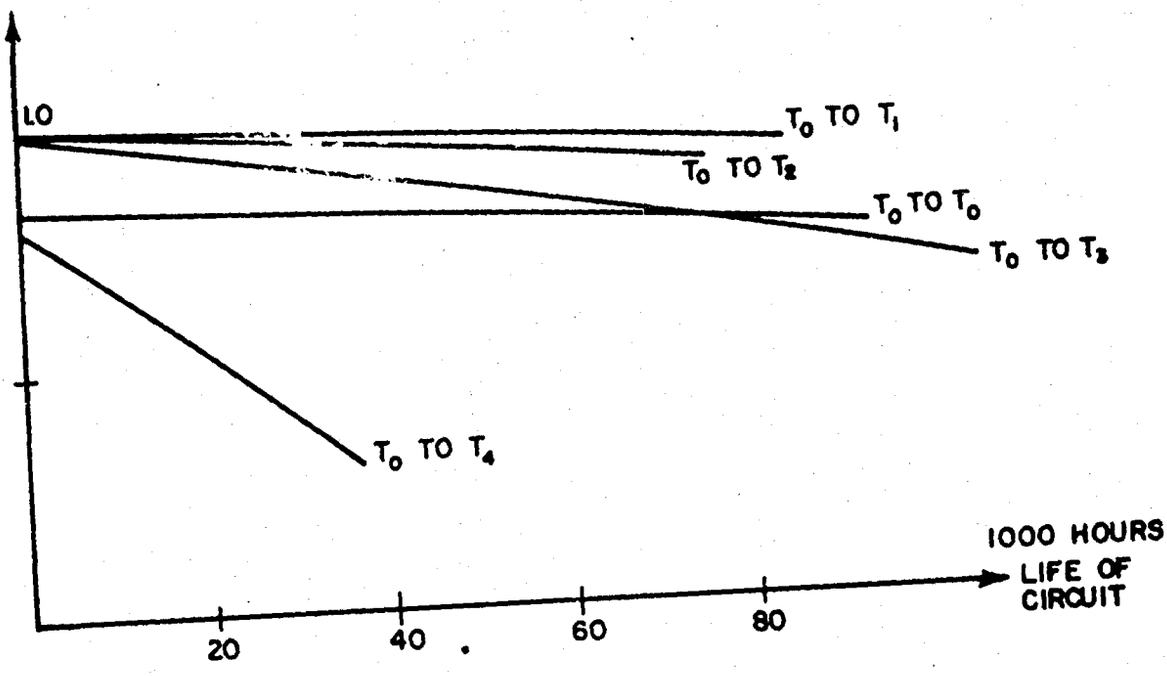
(m) Conclusions

It is from curves like those of Figure 7 that it may be decided which system is most reliable and when redundancy is necessary.

From the curves the following may be seen:

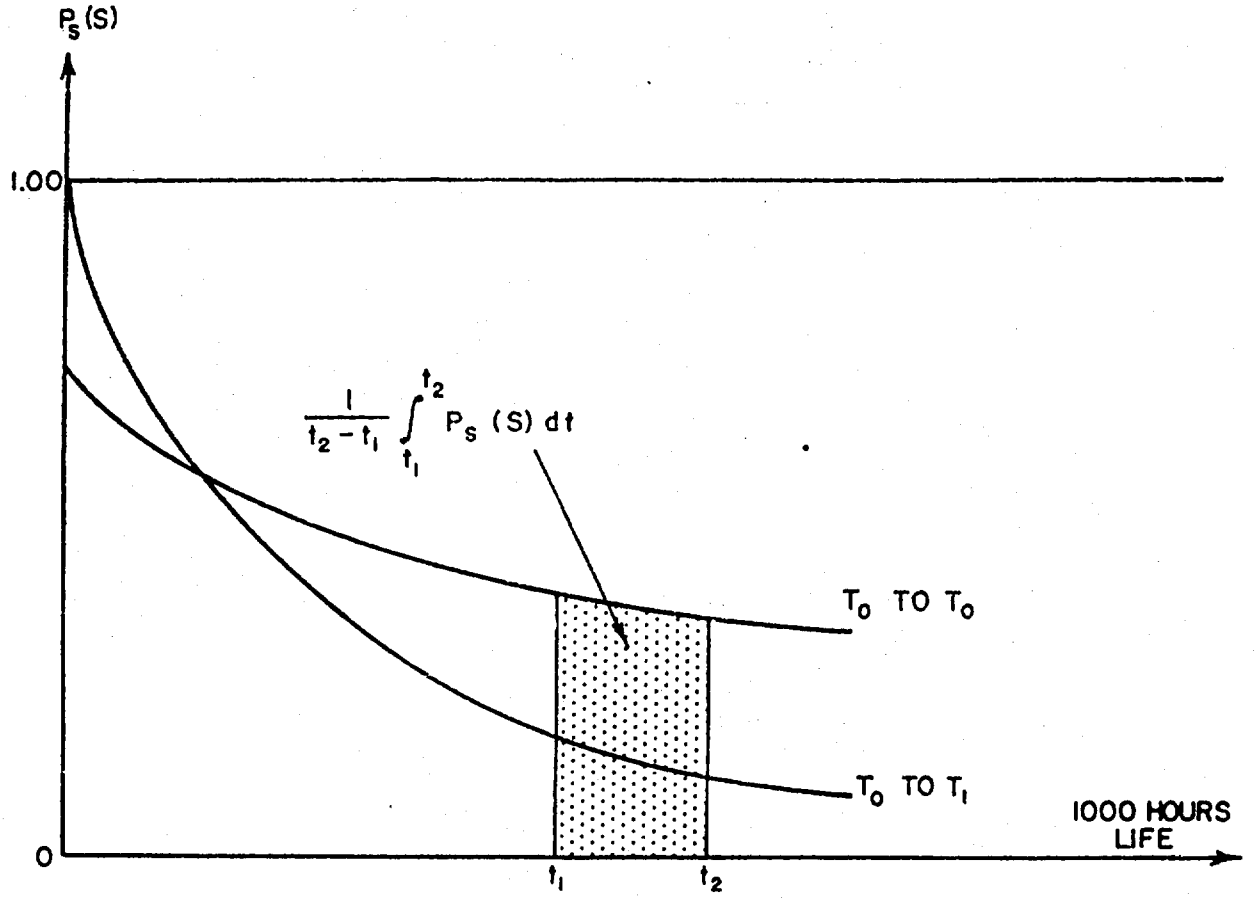
(1) If the circuit components have narrow tolerances, the worst case designed circuits will have smaller W-values (less power dissipation) and lower T_{op}. Lower T_{op} means a higher P(D)-value and a smaller λ, both of which tend to increase P(S), see Equation (2), and thereby $P_s(S)$. Thus, system reliability is increased by use of components with narrow tolerances.

(2) Both improved cooling and low packing density will reduce the value of the Constant in Equation (1) and thus lower T_{op} which is desirable, see Equation 1. After the circuits have been manufactured they are inspected. If each circuit is tested at its natural temperature, the $1 - P(S)_{t=0}$ circuits which do not work at t = 0 will be detected and discarded. The success-probability



P (S) FOR FIVE CIRCUITS; $P(S)=P(D)e^{-\lambda t}$. SUCH CURVES ARE OBTAINABLE FOR ALL THE TYPES OF CIRCUITS WHICH CONSTITUTE THE SYSTEM.

FIGURE 6



PROBABILITY THAT THE SYSTEM WILL NOT FAIL, $P_S(S)$, AS A FUNCTION OF THE SYSTEMS LIFETIME.

FIGURE 7

of each of the remaining circuits which are used in the system then is:

$$P(S) = P(D)\, e^{-\lambda t} / P(S)_{t = 0}$$

Thus testing of each circuit further increases the system reliability.

APPENDIX B-2

CIRCUIT DESIGN

PART A. THE DESIGN EQUATIONS AND THEIR SOLUTIONS

1A. $(I_{C2})_{max}$ and I_{CBO}

The following equations assume that transistor T_1 is turned off, and transistor T_2 is turned on, see Figure 1. Equation (1) expresses that the junction temperature is the sum of the ambient temperature and the temperature rise caused by the power-dissipation in the transistor. As the power dissipation goes up with increasing collector current, the decreasing $I_{C2\ max}$ is determined by Equation (1).

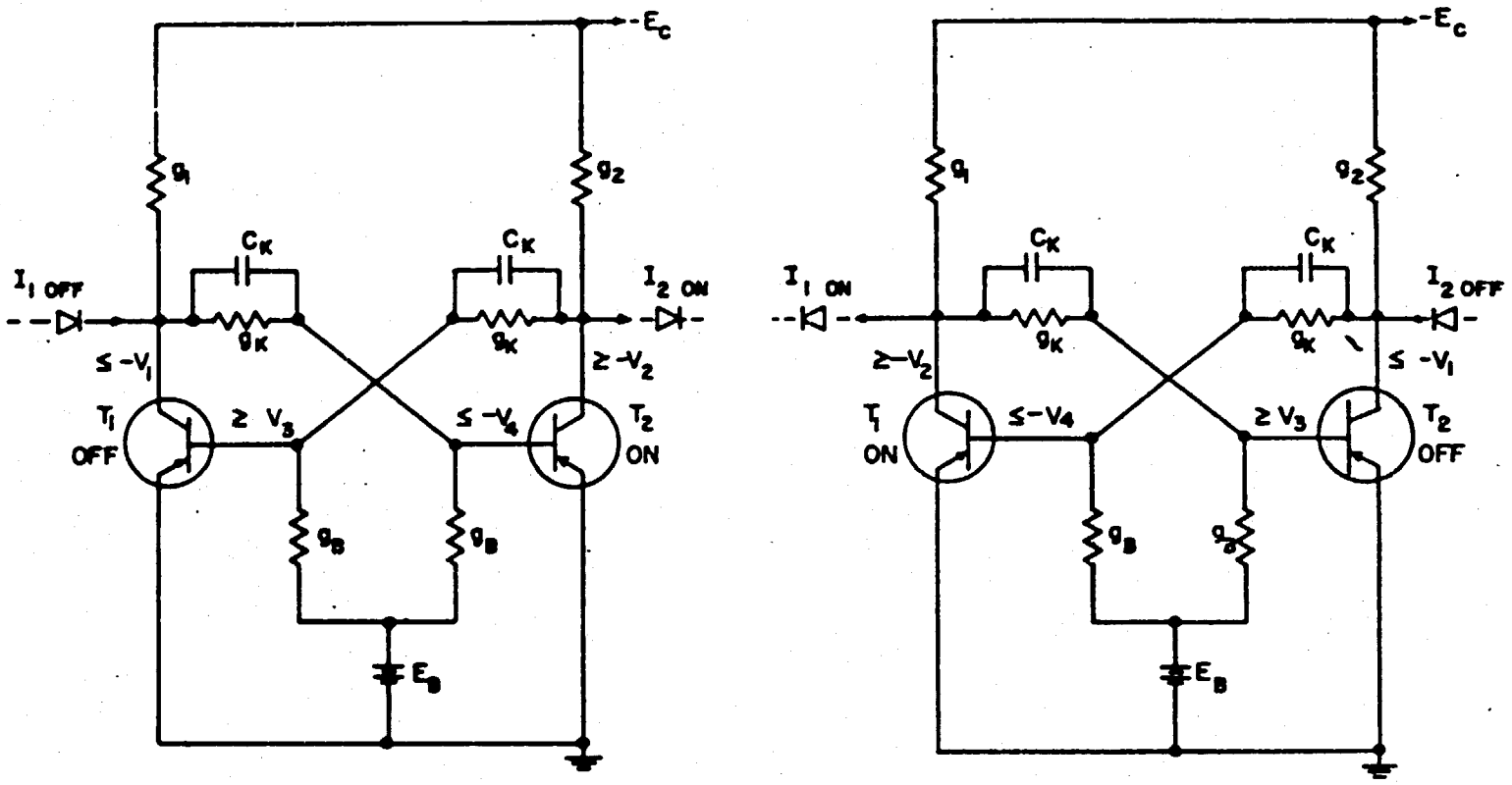
Equation (2) expresses that an 8°C increase in junction temperature will double the leakage current I_{CBO} of the turned-off transistor. This is a common rule of thumb. When a transistor has been driven with I_{C2} and then is turned off, in the first moment I_{CBO} will have its highest value. It is this value of I_{CBO}, we obtain from Equation (2). When I_{C2} is known, I_{CBO} is determined by (2).

$$T_{JUNCTION,\ MAX} = T_{AMB,\ MAX} + K \times V_2 \times (I_{C2})_{MAX}\ ; \qquad (1)$$

$$I_{CBO} = (I_{CBO,\ MAX})_{\text{ROOM TEMP, } -E_C} \times 2^{\left[\frac{T_{AMB,\ MAX} - T_{ROOM}}{8}\right]} \times \left[\frac{KV_2\ I_{C2}}{8}\right]\ ; \qquad (2)$$

1B. I_{C2} as Parameter

A typical beta versus collector current curve for the 2N396 transistor is shown in Figure 2. We will use I_{C2} as the dependent.



THE FLIP-FLOP IS SAID TO BE BISTABLE WHEN THE TWO REQUIREMENTS BOTH ARE MET:

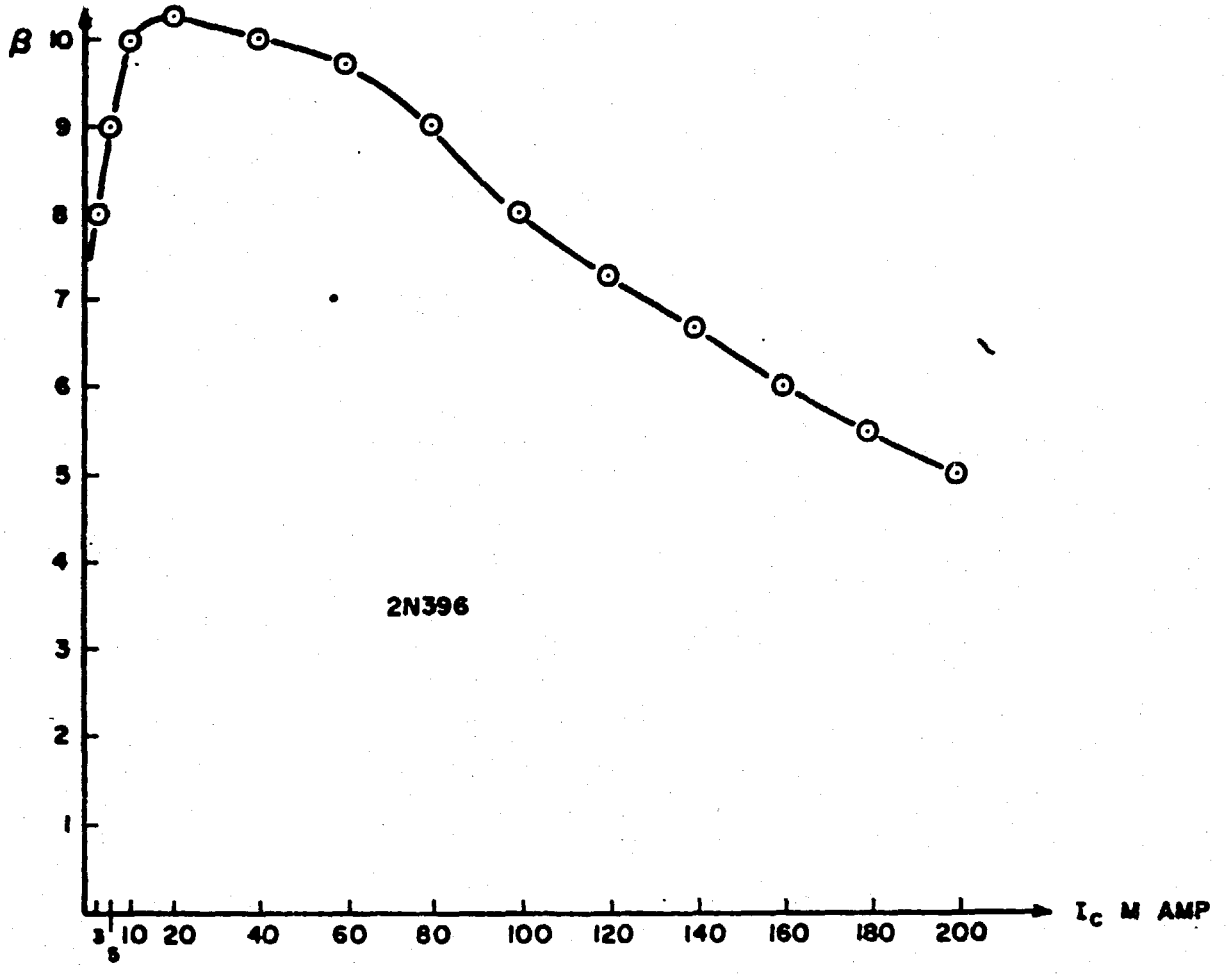
$V_{C1} \leq -V_1$, $V_{B1} \geq V_3$, $V_{C2} \geq -V_2$ AND $V_{B2} \leq -V_4$ FOR T_1 OFF AND T_2 ON,

$V_{C1} \geq -V_2$, $V_{B1} \leq -V_4$, $V_{C2} \leq -V_1$ AND $V_{B2} \geq V_3$ FOR T_1 ON AND T_2 OFF,

A TYPICAL SET VALUES IS $E_B = 5V$, $-E_C = -10V$, $-V_1 = -6V$, $-V_2 = -.1V$, $V_3 = .1V$ AND $-V_4 = -1V$.

A BASE RETURNED, SATURATING FLIP-FLOP IN ITS TWO STATES WITH LOAD CURRENTS.

FIGURE 1



TYPICAL VARIATION IN β WITH COLLECTOR CURRENT ; I_C 10 M AMPS USED AS REFERENCE. THE CURVE IS ONLY VALID FOR 2N396 WITH AN AMBIENT TEMPERATURE OF 25°C, AND V = .2 VOLTS

FIGURE 2

variable in the calculations of G_B, G_K, G_1 and G_2. I_{C2} is the current from T_2's collector when T_2 is turned on. This approach has the following advantages:

(a) $(I_{C2})_{MAX}$ may readily be calculated from Equation (1). Typical test values of I_{C2} called I_a, I_b, I_c, etc., are chosen and each is stored with the β_{min} value which corresponds to the current and to $V_{C2} = -V_2$. The minimum gain values are called β_a, β_b, β_c, etc. In this way we include β_{min}'s dependence on I_{C2} in our calculations.

(b) I_{C2} appears in the exponential expression for I_{CBO}, see Equation (2). The equation system (2), (3), (4), (5), (6) determine G_B, G_K, G_1, G_2, I_{CBO} and I_{C2} when one of the six values is known. By using I_{C2} as parameter, we avoid solving a transcendental equation.

Notice that the following inequalities which determine $(g_B, g_K, g_1, g_2) = (G_B, G_K, G_1, G_2)$ all refer to the flip-flop, figure 1, when unloaded.

1C. Inequality (3)

To keep T_1 turned off, the transistor must receive the base current I_{CBO}. See Figure 1. We assume $-V_2 = -V_4$. I_D is the largest current which will leak out at maximum ambient temperature through the trigger circuitry of the off-transistor. We assume that the trigger circuit is connected to the base of the transistor.

T_1 stays turned off when inequality (3) is satisfied. It will here be necessary to illustrate by an example the nomenclature used in the following: If a conductance (or supply voltage) has the nominal value g_B (or E_C) we will express the lower limit for the true value of the conductance (or supply voltage) as $g_B\ (\delta_{gB})_L$, or $E_C\ (\delta_{EC})_L$, and the higher limit for the true value as $g_B\ (\delta_{gB})_H$, or $E_C\ (\delta_{EC})_H$. $(\delta)_L$- values are usually less than 1. $(\delta)_H$ values are usually more than 1.

When the tolerances are taken into consideration, inequality (3a) has to be satisfied to keep T_1 turned off.

$$g_B \left[E_B - V_3\right] - g_k \left[V_3 + V_2\right] \geq I_{CBO} + I_D; \qquad (3)$$

$$g_B\,(\delta_{gB})_L\,(1/\delta_g) \left[E_B\,(\delta_{EB})_L - V_3\right] - g_K(\delta_{gK})_H \left[V_3 + V_2\right] \geq I_{CBO} + I_D; \qquad (3a)$$

1D. Inequality (4)

To keep T_2 turned on, the coupling conductance must accept at least the current of I_{C2}/β from T_2's base. This is expressed by inequality (4).

When the tolerances are taken into consideration, we will insist that the (conservative) inequality (4a) is satisfied. Notice that the inequalities (3) and (4), or (3a) and (4a) determine g_B and g_K. g_B and g_K are determined independently of g_1, g_2 and $-E_C$ as could be expected from circuit considerations.

$$-g_B \left[E_B + V_2\right] + g_K \left[V_1 - V_2\right] \geq \frac{I_{C2}}{\beta}; \qquad (4)$$

$$-g_B\,(\delta_{gB})_H\ (\delta_g) \left[E_B\,(\delta_{EB})_H + V_2\right] + g_K\,(\delta_{gK})_L \left[V_1 - V_2\right] \geq I_{C2}/\beta; \qquad (4a)$$

1E. Inequality (5)

The inequality shows the constraints imposed upon g_1, when V_{C1} should be kept less than $-V_1$. When g_K has been determined from (3) and (4), g_1 may be determined from (5).

When the tolerances are taken into account, inequality (5a) should be satisfied.

$$g_1 \left[E_C - V_1\right] - g_K\left[V_1 - V_2\right] \geq I_{CBO} \tag{5}$$

$$g_1 (\delta_g)_L \left[E_C (\delta_{EC})_L - V_1\right] - g_K (\delta_{gK})_H \left[V_1 - V_2\right] \geq I_{CBO} \tag{5a}$$

1F. Inequality (6)

We want to choose g_2 so that the parameter value of I_{C2} is the largest possible collector current from T_2.

If we do not design this way, the minimum I_{B2} which is capable of keeping T_2 turned on could be larger than the foreseen I_{C2}/β. When g_K is known, g_2 may be determined from (6).

Without tolerances, we obtain inequality (6). When the tolerances are taken into account, we arrive at inequality (6a).

$$g_2 \left[E_C - V_2\right] - g_K \left[V_3 + V_2\right] \leq I_{C2}\ ; \tag{6}$$

$$g_2 (\delta_g)_H \left[E_C (\delta_{EC})_H - V_2\right] - g_K (\delta_{gK})_L \left[V_3 + V_2\right] \leq I_{C2}; \tag{6a}$$

1G. Solving the Equation System

In this appendix we solve the problem of finding g_B, g_K, g_1 and g_2 from the five expressions (2), (3a), (4a), (5a) and (6a) for some value of the parameter I_{C2} and its associated β_{min}. The solution is called (G_B, G_K, G_1, G_2). It is assumed that the nineteen constants which appear in the five expressions all are known.

In this appendix we are not concerned about whether the four conductances are available values or not. We can therefore use the equal sign in the inequalities (3a), (4a), (5a) and (6a), and consider δ_g equal to 1. In this way we obtain the smallest conductance values.

The steps are as follows. Find I_{CBO} from (2). Find $(g_B, g_K) = (G_B, G_K)$ from (3a) and (4a). Find $g_1 = G_1$ from (5a). Find $g_2 = G_2$ from (6a). All four conductances obviously should be positive to make the flip-flop realisable. The five expressions therefore show the relationships between the nineteen constants which must be fulfilled to obtain realizable flip-flop configurations

There are four modes under which the program can operate:

1. Compute preferred conductances, and execute one design.

2. Compute preferred conductances, and execute more than one design.

3. Enter preferred conductances, and execute one design.

4. Enter preferred conductances, and execute more than one design.

The required input data differs among modes as will be described below.

First will be described the operation of the program under mode No. 1, since the remaining modes are the results of minor modifications of this mode.

Mode No. 1

The input data required for mode no.1 are listed below. They are grouped into three classes denoted A, B, and C, corresponding to the three classes of subscripted variables A(I), B(I), and C(I) by which they are identified in the program.

A(1) - A(40). Values of $\beta(I)$. In general, there will be fewer than 40 values; the exact number is given by one of the B(I) data, B(38).

B(1) - B(40). The meanings of these numbers are given below. B(1) and B(2) are not referred to in the program, but must be included as part of the input to maintain a proper format.

B (1)		Not used
B (2)		Not used
B (3)	E_cMin	= Minimum value of collector supply voltage
B (4)	E_cMax	= Maximum value of collector supply voltage
B (5)	E_BMin	= Minimum value of base return voltage
B (6)	E_BMax	= Maximum value of base return voltage
B (7)	V_T	= Minimum trigger amplitude
B (8)	V_T'	= Minimum slope of trigger pulse rise time
B (9)	V_1	= Minimum absolute difference between "OFF" collector voltage and ground
B(10)	V_2	= Maximum absolute difference between "ON" collector voltage and ground
B(11)	V_3	= Absolute value of V_{BE} when transistor starts to conduct
B(12)	V_{FD}	= Forward voltage drop of trigger diode
B(13)	I_{cBO}	= Maximum transistor leakage current at room temp. and end of life
B(14)	I_DMax	= Maximum diode leakage current at maximum ambient temp. and end of life
B(15)	I_1 on	= Maximum external load current at T_1 when the transistor is conducting
B(16)	I_1 off	= Maximum external load current at T_1 when the transistor is turned off
B(17)	I_2 on	= Maximum external load current at T_2 when the transistor is conducting
B(18)	I_2 off	= Maximum external load current at T_2 when the transistor is turned off
B(19)	$+\delta_{g+}$	= Maximum expected ratio conductance increase to nominal value at end of life and temp. extremes
B(20)	$+\delta_{g-}$	= Maximum expected ratio of conductance decrease to nominal value at end of life and temp. extremes

B(21)	$+\delta S/2_+$	= The average ratio of the difference between two adjacent standard conductance values divided by their sum
B(22)	$+\delta S/2_-$	
B(23)	$+\delta_{c+}$	= Maximum expected ratio of capacitance increase to nominal value due to tolerance, aging and temp.
B(24)	$+\delta_{c-}$	= Maximum expected ratio of capacitance decrease to nominal value due to tolerance, aging and temp.
B(25)	C_c	= Collector capacitance maximum, of the transistor type used in the circuit (common base)
B(26)	C_{L1}	= Load capacitance in shunt with collector of T_1
B(27)	C_{L2}	= Load capacitance in shunt with collector of T_2
B(28)	R_S	= Trigger generator source resistance
B(29)	F	= Maximum trigger rate at which the flip flop must operate (pulses per second)
B(30)	K	= Inverse of transistor derating factor (°C/WATT)
B(31)	T_A	= Maximum component part ambient temp. (°C)
B(32)	T_R	= Room temperature, normally 25°C
B(33)	$W\alpha_E$	= Common emitter cutoff frequency (rad./sec.)
B(34)	W_S	= Inverse of carrier storage factor (1/sec.)
B(35)	T_S	=
B(36)		= Number Res. Values
B(37)		= > 0 → call dump
B(38)		= Number β Values
B(39)		= pos → continue next design
B(40)		= neg → skip computation of preferred conductances

$$(2')\quad E(I) = B(13)\cdot EXP_2\left[\frac{B(31) + B(30)\cdot B(10)\cdot C(I) - B(32)}{8}\right]$$

$$(3)\quad \varepsilon_{K_1} = \left[\frac{I_{C_2}}{\beta}\right] i \left[(1 - \delta g)(1 - \delta s/2)(E_{B_{MIN}} - V_3)\right]$$

$$+ (1 + \delta g)(1 + \delta s/2)(E_{B_{MAX}} + V_2)\cdot(I_{CBO_{MAX_1}} + I_{D_{MAX}})$$

$$\div \left[(1 - \delta g)^2(1 - \delta s/2)(E_{B_{MIN}} - V_3)(V_1 - V_2)\right.$$

$$\left. - (1 + \delta g)^2\cdot(1 + \delta s/2)\cdot(V_2 + V_3)\cdot(E_{B_{MAX}} + V_2)\right]$$

$$(3')\quad Q(1,I) = \left[\frac{C(I)}{A(I)}\right]\cdot\left[(1 - B(20))(1 - B(22))\cdot(B(5) - B(11))\right]$$

$$+ (1 + B(19))\cdot(1 + B(21))\cdot(B(6) + B(10))\cdot(E(I) + B(14))$$

$$\div \left[(1 - B(20))^2\cdot(1 - B(22))(B(5) - B(11))(B(9) - B(10))\right.$$

$$\left. - (1 + B(19))^2\cdot(1 + B(21))(B(10) + B(11))\cdot(B(6) + B(10))\right.$$

B(39) and B(40) are negative for Mode No. 1 operation.

C(1) - C(40). Values of I_{C_2}. These are in one-to-one correspondence with A(1) - A(40); this correspondence gives β as a function of I_{C_2}.

ZRES(I), I = 1, B(36). These are the values of the lower decade of standard resistances that are to be used in the design. The next three higher decades of corresponding conductances are generated by the program, and the four decades held in memory.

Note that the number of values in one decade, and the number read into the program must be specified by the constant B(36). (This constant is relabeled IB in the program.)

In the description that follows, each equation is written twice, first using symbols which are used also in "Computer Design Programs" cited on page 1, and second using symbols assigned by the program; knowledge of this second set of symbols is necessary only if it is desired to investigate the contents of the memory after running a design.

I.

A. Compute a list of standard conductance values as noted above. These values are denoted by the subscripted variable G(I).

B. Compute

(1) $T_{MAX_i} = T_A + K \cdot V_2 \cdot I_{C_{2_i}}$

(1') $D(I) = B(31) + B(30) \cdot B(10) \cdot C(I)$

(2) $I_{CBO_{MAX_i}} = I_{CBO} \cdot EXP_2 \left[\dfrac{T_A + K \cdot V_2 \cdot I_{C_{2_i}} - T_R}{8} \right]$

IREP is set equal to the input constant B(38); the six expressions listed above are evaluated for I = 1,2,..., IREP.

C. Determine all standard conductance values between

(1) g_{K_i} and $g_{K_{i+1}}$

(1') Q(1,I) and Q(1,I + 1) for I = 1, IREP - 1 .

These values are denoted by

(2) $G_{K_{i1}}$, $G_{K_{i2}}$, ... etc.

In the program the set of values (2) are identified as the set of G(I)'s that range from G[K1(I)] through G[K2(I)] where the subscripts here correspond to the lower-case i's in (2).

D. Compute

(1) $$\frac{G_{K_{ij}} - g_{K_i}}{g_{K_{i+1}} - g_{K_i}}$$

(1') R(I,J) for I = 1, IREP - 1 J = K 1(I), K2(I) .

E. Compute

(1) $$g_{B_{ij}} = (g_{B_{i+1}} - g_{B_i}) \left[\frac{G_{K_{ij}} - g_{K_i}}{g_{K_{i+1}} - g_{K_i}} \right] + g_{B_i}$$

(1') $$S(2,I,J) = \left[Q(2,I + 1) - Q(2,I) \right] \left[\frac{G[K1(I) + J] - Q(1,I)}{Q(1,I + 1) - Q(1,I)} \right] + Q(2,I)$$

(4)

$$g_{B_i} = \frac{\left[\frac{I_{C_2}}{\beta}\right]_i \cdot \left[(1 + \delta g)(V_2+V_3)\right] + (1 - \delta g)(V_1 - V_2)(I_{CBO_{MAX_i}} + I_{D_{MAX}})}{\left[(1 - \delta g)^2(1 - \delta s/2)(E_{B_{MIN}} - V_3)(V_1 - V_2) - (1 + \delta g)^2 \cdot (1 + \delta s/2)(V_2 + V_3)(E_{B_{MAX}} + V_2)\right]}$$

(4')

$$Q(2,I) = \frac{\left[\frac{C(I)}{A(I)}\right] \cdot \left[(1 + B(19))(B(10)) + B(11)\right] + (1 - B(20))(B(9) - B(10))(E(I) + B(14)}{\left[(1 - B(20))^2(1 - B(22)(B(5) - B(11))(B(9) - B(10)) - (1 - B(19))^2 \cdot (1 + B(21))(B(10)+B(11))(B(6) + B(10))\right]}$$

(5)

$$g_{1_i} = \frac{I_{CBO_{MAX_i}} + I_{D_{MAX}} + (1 + \delta g)(V_1 - V_2) \cdot g_{K_i}}{(1 - \delta g)(E_{C_{MIN}} - V_1)}$$

(5')

$$Q(3,I) = \frac{E(I) + B(14) + (1 + B(19))(B(9) - B(10)) \cdot Q(1,I)}{(1 - B(20)) \cdot (B(3) - B(9))}$$

(6)

$$g_{2_i} = \frac{I_{C_{2_i}} + (1 - \delta g)(V_2 + V_3) g_{K_i}}{(1 + \delta g)(E_{C_{MAX}} - V_2)}$$

(6')

$$Q(4,I) = \frac{C(I) + (1 - B(20))(B(10) + B(11)) \cdot Q(1,I)}{(1 + B(19))(B(4) - B(10))}$$

to be called in the program

(3') [G(J), T(J), SN(3,J), SN(4,J)] .

G. The entire list of preferred conductance sets, (3'), is printed out, i = 1, IREP, j = K1(i), K2(i) .

II.

A. Compute

(1) $$\Delta g_1 = \left| \frac{I_{1_{ON}}}{E_{C_{MIN}} - V_2} - \frac{I_{1_{OFF}}}{E_{C_{MIN}} - V_1} \right|$$

(1') $$D\,1 = \left| \frac{B(15)}{B(3) - B(10)} - \frac{B(16)}{B(3) - B(9)} \right|$$

(2) $$\Delta g_2 = \left| \frac{I_{2_{ON}}}{E_{C_{MIN}} - V_2} - \frac{I_{2_{OFF}}}{E_{C_{MIN}} - V_1} \right|$$

(2') $$D\,2 = \left| \frac{B(17)}{B(3) - B(10)} - \frac{B(18)}{B(3) - B(9)} \right|$$

The first conductance set

(3) $$\left[G_{K_{ij}}, G_{B_{ij}}, g_{1_{ij}}, g_{2_{ij}} \right]$$

(3') $$\left[G(J), T(J), SN(3,J), SN(4,J) \right]$$

(2)

$$g_{1_{ij}} = (g_{1_{i+1}} - g_{1_i}) \left[\frac{G_{K_{ij}} - g_{K_i}}{g_{K_{i+1}} - g_{K_i}} \right] + g_{1_i}$$

(2')

$$S(3,I,J) = (Q(3,I+1) - Q(3,I)) \left[\frac{G[K1(I) + J] - Q(1,I)}{Q(1,I+1) - Q(1,I)} \right] Q(3,I)$$

(3)

$$g_{2_{ij}} = (g_{2_{i+1}} - g_{2_i}) \left[\frac{G_{K_{ij}} - g_{K_i}}{g_{K_{i+1}} - g_{K_i}} \right] + g_{2_i}$$

(3')

$$S(4,I,J) = (Q(4,I+1) - Q(4,I)) \left[\frac{G[K1(I) + J] - Q(1,I)}{Q(1,I+1) - Q(1,I)} \right] + Q(4,I)$$

for I = 1, IREP - 1, J = K1(I), K2(I)

F. Determine standard conductance, G(I), closest to

(1) $g_{B_{ij}}$

(1') S(2,I,J)

Denote this as

(2) $G_{B_{ij}}$

(2') T(K)

There are intermediate stages of computation involving changes of variable which cause the sets

(3) $\left[G_{K_{ij}}, G_{B_{ij}}, g_{1_{ij}}, g_{2_{ij}} \right]$.

(4') $$E6 = E3 + \frac{B(18)}{B(3) - B(9)} \quad .$$

Select the next larger standard conductance,

(5) y

(5') YL

such that

(6) $$y > g_{1_{a,b}} + \frac{I_{2_{OFF}}}{E_{C_{MIN}} - V_1}$$

(6') $$YL > E6$$

C. Check that

(1) $$x + \frac{I_{1_{ON}}}{E_{C_{MIN}} - V_2} < g_{2_{a,b}}$$

(1') $$XL + \frac{B(15)}{B(3) - B(10)} < E4 \quad .$$

If not, return to II,A,(3) above, and use the next larger conductance set. Otherwise

D. Check that

(1) $$y + \frac{I_{2_{ON}}}{E_{C_{MIN}} - V_2} < g_{2_{a.b}}$$

(1') $$YL + \frac{B(17)}{B(3) - B(10)} < E4 \quad .$$

for which $g_{2_{ij}} - g_{1_{ij}}$ is greater than both Δg_1 and Δg_2 is chosen, and denoted by

(4) $$\left[G_{K_{a,b}}, G_{B_{a,b}}, g_{1_{a,b}}, g_{2_{a,b}} \right]$$

(4') [E 1, E 2, E 3, E 4]

B. Compute

(1) $$g_{1_{a,b}} + \frac{I_{1_{OFF}}}{E_{C_{MIN}} - V_1}$$

(1') $$E5 \leftarrow E3 + \frac{B(16)}{B(3) - B(9)} \quad .$$

Select the next larger standard conductance,

(2) x

(2') XL

such that

(3) $$x > g_{1_{a,b}} + \frac{I_{1_{OFF}}}{E_{C_{MIN}} - V_1}$$

(3') XL > E5 .

Compute

(4) $$g_{1_{a,b}} + \frac{I_{2_{OFF}}}{E_{C_{MIN}} - V_1}$$

The values

(9) G_B and G_K

(9') EPG(3) and EPG(4)

are those values of $G_{B_{ij}}$ and $G_{K_{ij}}$ in that conductance set

$$\left[G_{K_{ij}}, G_{B_{ij}}, g_{1_{ij}}, g_{2_{ij}} \right]$$

which fulfilled all the above requirements.

III

A. Determine that value of I for which

(1) I_C

(1') C(I)

is nearest but equal to or greater than the larger of

(2) $E_{C_{MAX}} \quad (1 + \delta g) \cdot x$

(2') $B(4)(1 + B(19)) \cdot EPG(1) = D7$

and

(3) $E_{C_{MAX}} \quad (1 + \delta g) \cdot y$

(3') $B(4) \cdot [1 + B(19)] \cdot EPG(2) = D8$

Let

(4') $D9 = MAX\ (D7, D8)$

From the input data determine the corresponding value of β

(5') A(I)

If not, return to II, A, (3) above, and use the next larger conductance set. Otherwise

E. Compute and print out the last

(1) x

(1') EPG(1)

(2) $R_{L_1} = 1/x$

(2') $EPR(1) = \frac{1}{XL}$

(3) y

(3') EPG(2)

(4) $R_{L_2} = 1/y$

(4') $EPR(2) = \frac{1}{YL}$

(5) G_B

(5') EPG(3) = E2

(6) $R_B = \frac{1}{G_B}$

(6') $EPR(3) = \frac{1}{E2}$

(7) G_K

(7') EPG(4) = E1

(8) $R_K = \frac{1}{G_K}$

(8') $EPR(4) = \frac{1}{E1}$

C. Compute

(1) $\frac{2}{x}$

(1') $\frac{2}{EPG(1)} = RTM1$

and

(2) $\frac{2}{y}$

(2') $\frac{2}{EPG(2)} = RTM2$

Let

(3) $R_{T_{MIN}} = MAX\left(\frac{2}{x}, \frac{2}{y}\right)$

(3') $RTS = MAX(RTM1, RTM2)$

and compute

(4)

$$C_{T_{MIN}} = \frac{V_1 \cdot G_K - E_B G_B}{(1 - \delta_c)V_T'} + \frac{1}{(1 - \delta_c)\cdot 95(V_T - V_{FD} - V_3)}\left[\frac{I_C}{\beta W_{\alpha_E}} + \frac{V_1 G_K - E_B G_B - \frac{I_C}{\beta}}{W_s}\right]$$

(4')

$$CTM = \frac{B(9)\cdot EPG(4) - B(5)\cdot EPG(3)}{(1 - B(29))\cdot B(8)} + \frac{1}{(1 - B(29))\cdot 95(B(7) - B(12) - B(11)}$$

$$\left[\frac{C(IBETA)}{A(IBETA)\cdot B(33)} + \frac{B(9)\cdot EPG(4) - B(5)\cdot EPG(3) - \frac{C(IBETA)}{A(IBETA)}}{B(34)}\right]$$

B. Compute

(1) $$C_{K_{MAX}} = \frac{1}{3F}\,(G_B + \mathbf{Q}_K)$$

(1') $$CK1 = \frac{1}{3 \cdot B(29)}\,(E2 + E1)$$

(2) $$E_{K_{MIN_1}} = \frac{I_C}{\beta W_{\alpha_E} \cdot V_1} + C_c + \frac{C_{L_1}}{\beta}$$

(2') $$CK21 = \frac{C(I)}{A(I) \cdot B(33) \cdot B(19)} + B(25) + \frac{B(26)}{A(I)}$$

(3) $$C_{K_{MIN_2}} = \frac{I_C}{\beta W_{\alpha_E} \cdot V_1} + C_c + \frac{C_{L_2}}{\beta}$$

(3') $$CK22 = \frac{C(I)}{A(I) \cdot B(33) \cdot B(9)} + B(25) + \frac{B(27)}{A(I)}$$

check that

(4) $$C_{K_{MAX}} < MAX\,(C_{K_{MIN_1}}, C_{K_{MIN_2}})$$

(4') $$CK1 < MAX\,(CK21, CK22) = CK2 \quad .$$

If not, return to II, A, (3) above, and select the next larger conductance set. Otherwise, print out

(5) $$C_{K_{MAX}}, C_{K_{MIN}}$$

(5') $$CK1, \quad CK2 \quad .$$

Mode No. 3 operation is signalled in the input data by

a. $B(40) \leq 0$, which causes the computation of preferred conductances to be skipped.

b. $B(39) \leq 0$, which indicates that only one design is to be executed.

The sequence in which input data is entered is identical to that for Mode No. 1 except that the following data is added:

1. One card with a number which indicates the number of preferred conductance sets that are to be read in. This number is called KT in the program.

2. The preferred conductance sets on the appropriate number of cards in the following order:

   i. KT values of g_{k_i}, 3/card

   ii. KT values of g_{B_i}, 3/card

   iii. KT values of g_{1_i}, 3/card

   iiii. KT values of g_{2_i}, 3/card

These numbers are called in the program G(J), T(J), SN(3,J), and SN(4,J), respectively.

Mode No. 4

The program used in this mode operates identically with the operation described under Mode No. 3 except that more than one design is executed. This is again signalled by setting $B(39) > 0$ in each set of B(I)'s read in except the last.

$$(5) \qquad R_{T_{MAX}} = \frac{4}{F(1.2)(1+\delta_c)^2 C_{T_{MIN}}} - R_S$$

$$(5') \qquad RTB = \frac{4}{B(29)(1.2)(1+B(23))^2 \cdot CTM} - B(28)$$

Check that

$$(6) \qquad R_{T_{MAX}} < R_{T_{MIN}}$$

$$(6') \qquad RTB < RTS$$

and print out whether or not (6) is satisfied.

Mode No. 2

The input data is the same as in Mode No. 1, except

1. B(39) is made positive.
2. Added to the input data described under Mode No. 1 are additional sets of values for B(1) - B(40), in the same format as in Mode No. 1, for each additional design that is to be executed with the preferred conductances that have been computed the first time through the program. Each B(39) is made positive except the one in the set for the last design.

Mode No. 3

The program used in this mode does not compute a set of preferred conductances, but rather takes as part of its input data preferred conductances that have already been computed. In this mode only one design is executed.

Note that the format for all input data can be determined from the appropriate format statement in the Fortran listing.

APPENDIX B-3

CIRCUIT ANALYSIS

A. Introduction

A computer program is described here that performs the statistical analysis for determining the probability of drift failure for flip-flop circuits. The method of computation is the model-sampling or "Monte Carlo" whereby circuits, previously designed (see Appendix B-2), are tested by means of several criteria for satisfactory performance. The ratio of failures to the number of trials is used as the estimate of the probability of drift failure for the circuits.

Static performance of the circuits is judged satisfactory if each of the following six inequalities is satisfied; unsatisfactory otherwise.

$$\frac{V_1-V_4}{R_K} \geq \frac{I_{C2}}{\beta} + \frac{E+V_4}{R_B} \tag{1}$$

$$\frac{E-V_3}{R_B} \geq I_{CBO1} + I_D + \frac{V_3+V_2}{R_K} \tag{2}$$

$$\frac{E_C-V_1}{R_{10}} \geq I_{CBO1} + I_{1OFF} + \frac{V_1-V_2}{R_K} \tag{3}$$

$$\frac{V_1-V_4}{R_K} \geq \frac{I_{C1}}{\beta} + \frac{E+V_4}{R_B} \tag{4}$$

$$\frac{E-V_3}{R_B} \geq I_{CBO2} + I_D + \frac{V_3+V_2}{R_K} \tag{5}$$

$$\frac{E_C-V_1}{R_{20}} \geq I_{CBO2} + I_{2OFF}\,\frac{V_1-V_2}{R_K} \tag{6}$$

The first three inequalities are for the flip-flop state, transistor T_1 off and transistor T_2 on. The latter three inequalities are for the flip-flop state transistor T_1 on and transistor T_2 off.

The following equations are used to determine the constants I_{CX}, $I_{CX/\beta}$ and I_{CBOX} where X equals 1 for computations involving inequalities (1), (2) and (3) and X equals 2 for computations involving inequalities (4), (5), and (6).

$$I_{CX} = I_{XON} + \frac{E_C - V_2}{R_{20}} - \frac{V_3 + V_2}{R_K} \quad \ldots \; (X = 1 \text{ or } 2) \tag{7}$$

$I_{CX/\beta}$ select from (I_C, β) curve of Figure . (8)

$$I_{CBOX} = \left[(I_{CBO,MAX}) \; T_{ROOM} \text{AND} - E_C \right] \left[\frac{T_{AMB,MAX} - T_{ROOM}}{2 \quad D^\circ} \right]$$

$$\left[\frac{KV_2 I_{CX}}{2 \quad D^\circ} \right] \quad \ldots \; (X = 1 \text{ or } 2) \tag{9}$$

The program treats the six quantities

E_C

E

R_B

R_K

R_{10}

R_{20}

in the above equations as random variables. In the following discussion these random variables are denoted y_i, $i = 1,2, \ldots,6$.

The y_i's are each distributed uniformly and symmetrically about nominal values which we will denote by x_1, $i = 1,2,\ldots,6$. These nominal values plus the widths of the distributions, which we will denote by PC_1, a fraction (of x_1), are part of the input data.

The program provides the facility for skewing each of the above distributions for the purpose of reducing the variance of the sampled estimate of

failure probability.

Each of the skewed distributions is defined by the four parameters x_i, PC_i, a_i, and b_i. The latter two have the following meaning.

Each skewed distribution can be written

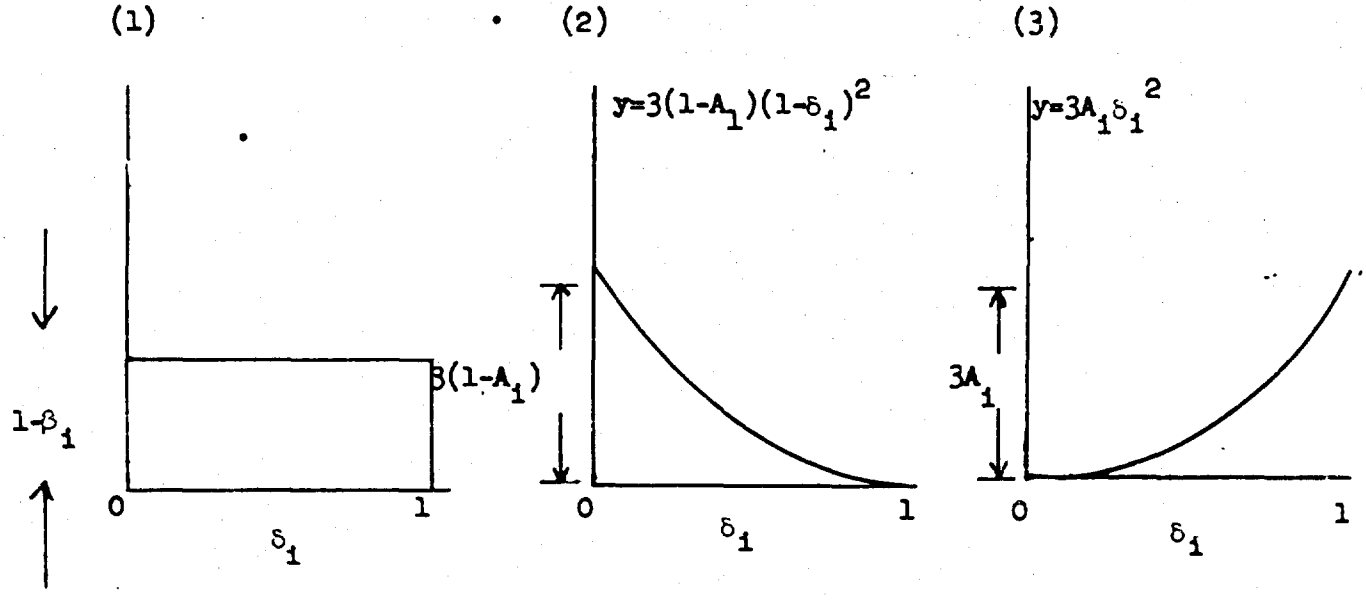
$$y_i = x_i \left[1 - \frac{PC_i}{2} \right] + \delta_1 \, PC_i \, x_i \qquad (10)$$

where δ_i is a random variable with a p.d.f. given by

$$p(\delta_i) = 3 \left[A_i B_i \, \delta_i^2 + (1-A_i)(1-\delta_i)^2 \right] + (1-B_1) \qquad (11)$$

$$0 \leq a_i \leq 1, \; 0 \leq b_i \leq 1$$

Thus, the skewed distribution is bi-modal, the lower peak being weighted by $(1 - A_i)$, the upper by A_i. A bias of $(1 - B_i)$ is provided across the entire distribution. In sum, the final distribution is the sum of the following three functions:



The values of A_i and B_i are chosen for minimum sampling variance as later described.

As a computational convenience in the program the above distribution is obtained as follows. If RN (this will denote a random number selected from a flat distribution in (0,1)) is less than $(1 - B_i)$, another RN is chosen (call this δ_i). Otherwise, a second RN is chosen. If this number is less than $(1 - A_i)$, δ_i is taken as the minimum of three additional RN's, otherwise as the maximum of the three RN's. (It is easy to check that $(n - 1) X^n$ is the p.d.f. of the maximum of n independent samples of a random variable uniformly distributed in the unit interval.)

It is implicit in the preceding that the random variable y_i, i= 1,2, ...,6 are independent, and this assumption is made throughout. Thus the joint distribution of the y_i's, say

$$p(y_1, y_2, \ldots, y_6) = p(\vec{y})$$

can be written

$$p(\vec{y}) = \prod_{1}^{6} p_i(y_i)$$

where $p_i(y_i)$ is the p.d.f. of the i^{th} random variable.

Now if these distributions were not disturbed in the sampling -- i.e., each remaining rectangular -- then, if $F_j = 0$ were to denote satisfaction of the inequalities (1) - (6) for the j^{th} circuit randomly constructed, and $F_j = 1$ denoted failure of at least one inequality, an estimate of the probability of failure of the circuit would be provided by

$$p(\tilde{f}) = \frac{1}{N} \sum_{j=1}^{N} F_j \qquad (12)$$

where N represents the number of trials (circuits tested).

Since, however, the distributions have been altered from $p_i(y_i)$ to, say, $p_i'(y_i)$, a proper estimate of p(f) will be provided by

$$\tilde{p}(f) = \frac{1}{N} \sum_{j=1}^{N} \frac{F_j P(\vec{y})}{p'(\vec{y})}$$

where $P'(\vec{y}) = \pi_1^6 p_1'(y_i)$.

Furthermore, the inequalities do not each involve all six random variables, so that if an inequality is dissatisfied $p(\vec{y})$ and $p'(\vec{y})$ in (13) are taken to be the joint p.d.f.'s of only those random variables in the inequalities so far tested. This technique causes the sampling variance to be less, clearly, than if all random variables were used.

Note: As a matter of terminology, those simulated failures which occur as a consequence of sampling from the skewed distributions will be referred to as pseudo-failures. This same terminology is used in the output format of the program.

B. Skewing of Sampling Distributions

The program has been designed so that appropriate modifications of the sampling distributions can be made between runs. Thus, successively smaller sampling variances are encountered. The modifications are made on the basic of the following statistics computed in each run.

a. The number of times the i^{th} inequality is tested (this will be, in general, less than the total number of trials, since the inequalities are tested sequentially, and if one fails those that follow are not tested).

b. The number of times the i^{th} inequality fails (note that this number divided by the number of times the i^{th} inequality is tested is not an estimate of the probability of the pseudo-failure of the i^{th} inequality, since the i^{th} inequality is tested only conditioned on those already tested being satisfied).

c. The average of y_i given that the j^{th} inequality fails.

d. The average amount by which the i^{th} inequality is dissatisfied; the average amount by which the i^{th} inequality is satisfied.

e. Total number of pseudo-failures, and, equivalently, the probability of a pseudo-failure.

f. The sample variance and standard deviation of the probability of failure.

C. The Sample Probability of Failure

It should be noted that the variance computed in f, and appearing in the print-out, is the estimated variance of the random variable corresponding to a single sample. The mean of N of these samples, where N is the total number of trials, is the number computed in (g), and the variance of this is $\frac{1}{N}$ th of that estimated in (f).

The procedure for modifying the distributions $p_i(y_i)$ on the basis of the above computations is not a formal one. The direction of required changes of each A_i, B_i is usually clearly indicated.

Briefly, if the expected value of a function which takes on only the values zero or one is being estimated, the (skewed) sampling distribution should be made to favor the one values of the function as much as possible (and at the same time as evenly as possible). Thus, the A_i and B_i parameters should be so

Best Available Copy

modified as to skew the $p_i(y_i)$ distributions toward the failure regions. The program outputs are designed to guide the changes made in these parameters.

D. The Program Computes and Stores 1600 Values of the Following

Fortran Designation	Description
TRB1	True value of R_{B1}
TRB2	True value of R_{B2}
TRK1	True value of R_{K1}
TRK2	True value of R_{K2}
TRX	True value of R_{10}
TRXX	True value of R_{20}
TREC	True value of E_C
TREB	True value of E_B
DF1	Difference in 1st inequality
DF2	Difference in 2nd inequality
DF3	Difference in 3rd inequality
DF4	Difference in 4th inequality
DF5	Difference in 5th inequality
DF6	Difference in 6th inequality

Also computes the following:

Fortran Designation	Description
CA	Random number
P	Probability of Failure for each random value at a given inequality.
AA	1.-A (see input)
BB	1.-B " "

Fortran Designation	Description
HH	A 6 x 20 MATRIX Giving averages of true values for resistors and voltages. 1-10 are averages if circuit failed, 10-20 are averages if successful.
PPF	Pseudo probability of failure
TPF	True probability of failure
VAR	Variance
STD	Standard deviation

Input Constants are Required as Follows:

RN	An initializing number for the random no. generator.
N1	The number of trials for a run on each flip-flop.
AK	A constant K used to compute ICB01 and ICB02.
AI1N	I_{1ON}
AI2FO	I_{2OFF}
AI2N	I_{2ON}
AI1FO	I_{1OFF}
DUM	+ or 0 gives P dump, - skips P dump
V1	
V2	Voltage level between 2 points in the flip-flop.
V3	
V4	
AID	I_D
AICBO	I_{CBO} (MAX at T_R)

Fortran Designation	Description
TA	TA; temperature, ambient
TR	TR; " , room
DG	D(I_{CBO} doubles when junction temp. is increased by D°).
N3	A number from 1-5 indicating 1-5 different distributions to be used.
DRBL	Lower limit of the R_B dist.
DRBH	Higher " " " " "
DRKL	Lower limit of the R_K dist.
DRKH	Higher " " " " "
DRXL	Lower limit of the R_{10} dist.
DRXH	Higher " " " " "
DRXXL	Lower limit of the R_{20} dist.
DRXXH	Higher " " " " "
DECL	Lower limit of the E_C dist.
DECH	Higher " " " " "
DEBL	Lower limit of the E_B "
DEBH	Higher " " " " "
N2	No. of sets of nominal values for resistances and voltages.
RB	Nominal resistance of R_{B1} and R_{B2}
RK	" " " R_{K1} and R_{K2}
RX	" " " R_{10}
R_{XX}	" " " R_{20}
EC	" Voltage E_C
EB	" " E_B

Fortran Designation		Description
A		Value of A to skew distribution of Rand Nos.
B		Value of B to " " " Rand Nos.
AIS2		Values of I_{C2} from I_{C2} - BETA curve
BI		Values of Beta from I_{C2} -BETA curve
	Note: A152	Values must be read in with smallest value first and progressively larger values following.

The program generates a series of random numbers which are used as multipliers to get a random distribution of true resistor and voltage values between the upper and lower limits set in advance. This distribution can be linear or can be skewed to get a large proportion of the true values to be concentrated at either the high or the low limit or both.

A set of values for 6 resistors and 2 voltages are picked and calculations are made to see if the flip-flop will work. Six different inequalities must be satisfied for success. A violation of any one of the (6) will be a failure. When a failure occurs, the random number and constant used to determine the true value of resistance or voltage in the inequality that failed are put in the equation

$$P_i = 3\ (A_i \times B_i \times (RN)^2 + (1 - A_i) \times (1 - RN)^2) + (1 - B_i) \qquad (14)$$

using the P_i values we find

$$DUMA = 1/(P_1)(P_2) \ldots (P_n)$$

The cumulative sum of DUMA is stored and is called SDUMA. SDUMAS = $(DUMA)^2$ is also accumulated. After all N1 sets of values have been used pseudo probability

of failure (PPF) is found by dividing the number of times failure occurred (L - LC) by number of trials (L) (L actually = N1 and is MAX of 1600)

$$PPF = (L - LC)/L$$

True probability of failure (TPF) is found = SDUMA ÷ N1

Variance (VAR) is found = SDUMAS ÷ N1 - $(TPF)^2$

Sigma (STD) is found = $(VAR)^{1/2}$

This is repeated for N2 flip-flops ($N2 \leq 10$).

Then the resistor and voltage tolerances are changed and (N2) flip-flops evaluated again. There can be N3 sets of tolerances ($N3 \leq 5$).

NOTE A(1) & B(1) are skewing constants for RB1
A(2) & B(2) " " " " RB2
A(3) & B(3) " " " " RK1
A(4) & B(4) " " " " RK2
A(5) & B(5) " " " " R_{10}
A(6) & B(6) " " " " R_{20}
A(7) & B(7) " " " " E_C
A(8) & B(8) " " " " E_B

E. Input Data

The first series of data cards are to be read by a subroutine called READH (read header). The constants RN, N1, AK, AI1N, AI2FO, AI2N, AI1FO, DUM, V1, V2, V3, V4, AID, AICBO, TA, TR & DG are read by READH. All constants except N1 are floating point. Data to be read by READH start in column 7 on an IBM card and must not go beyond column 72. A blank must be left between the end of one constant and the start of the next. Floating point numbers must have a decimal point and fixed point numbers must be preceded by a comma and have no

decimal point. After the last constant an asterisk must be punched to indicate the end of the data for this routine.

The next data cards will contain data for values of N3, DRBL, DRBH, DRKL, DRKH, DRXL, DRXH, DRXXL, DRXXH, DECL, DECH, DEBL, & DEBH. 1 ≤ N3 ≤ 5 and its value is the number of sets of limits that are to follow for B, K. X, XX, EC, EB. DRBL & DRBH are the low & high limits of deviation from nominal for resistors B1 & B2. If the limits were .95 to 1.10% of nominal, DRBL would = -.05 & DRBH would = +.10. Under unusual temperature conditions both limits might have the same sign and may be so entered. This data is read in by a read input tape command with an (16/(12E6.4)) format. The data should be placed on the card in 6 column spaces; N3 is a fixed point number and its value will be put on 1st card in column 6 with no decimal point. On the next card will be the value of DRBL (1) which must be in the field of column 1 to 6, must have a decimal point and if negative must have a sign; following this in columns 7 to 12 will be value of DRBH (L) etc., until value of DEBH (1) has been read in. This value will go in Col's 66-72 of second card. If N3 was more than 1, a set of values will follow starting with DRBL(2) etc. No asterisk follows the last bit of data.

The next block of data starts on a new card and gives values of N2, RB, RK, RX, RXX, EC & EB. It is read by a read input tape command with an (I12/6E12.4) format. The value of N2 must have its last digit on list card in column 12 and have no decimal point; RB(1) on 2nd card must be in columns 1-12, RK(1) in col's 13-24, etc. Similar to preceding data ($1 \leq N2 \leq 10$).

The next block is the A & B data. This has a 12 column format. The value of A(1) in col's 1-12, B(1) in col's 13-24, A(2) in col's 1-12 of second card, etc. All values are floating point.

Similarly, the next block is the AIS2 & BI values which are in a 12 column format. Starting a new card, AIS2 (1) must be in col 1 to 12, BI(1) in columns 13 to 24, AISA(2) in col 1 to 12 of 2nd card, etc. All values are floating point and the set must total 15 cards.

PARAMETER CONFIDENCE DESIGN METHOD

1. Introduction

This section will describe a proposed novel design procedure intended to yield the most reliable circuit design for any arbitrary system application. The procedure is characterized by a unified approach inter-relating the design of realizable circuits; the relevant system considerations; and the explicit effect of system characteristics on the choice of the optimum realizable circuit design for the given system.

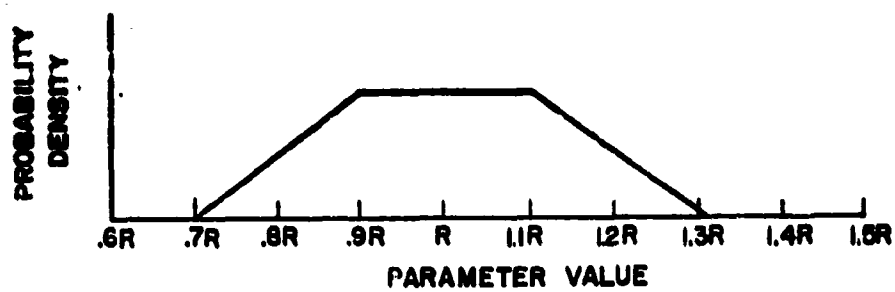
This design procedure presumes the following: a digital circuit application which involves a fixed number of building blocks of a fixed topology with a maximum required frequency of operation and a specified fan-in-fan-out requirement; a fixed mechanical packaging scheme which is to contain the fixed number of building blocks; and specific component types to be used in the circuits (e.g. a particular type of 5% resistors, 2N914 transistors, etc.). The result of the design is the selection of the nominal values of the designable parameters and/or to maximize the component yield.

a. The Parameter Confidence Limits and Interval

At the top of Figure 1, there is shown a probability density function for a hypothetical resistor type. The bottom of the figure shows the probability distribution for the same resistor type. The distribution curve is, of course, the integral from left to right of the density function. For this particular distribution, one would expect 10% of the parameter values to be less than 0.83 R and 90% to be less than 1.17 R. This is equivalent to saying that 80% of the values would be expected to be greater than 0.83 R but less than 1.17 R.

In the terminology of statistics, the limits which contain a parameter with a probability of 80% (or some other particular percentage) are called the 80% (or other) "confidence limits" for the parameter. The interval of parameter values between the confidence limits is called the "confidence interval". In this report, we will also speak of "degree of confidence" represented by Δ. Thus in Figure 1, the parameter values

Best Available Co



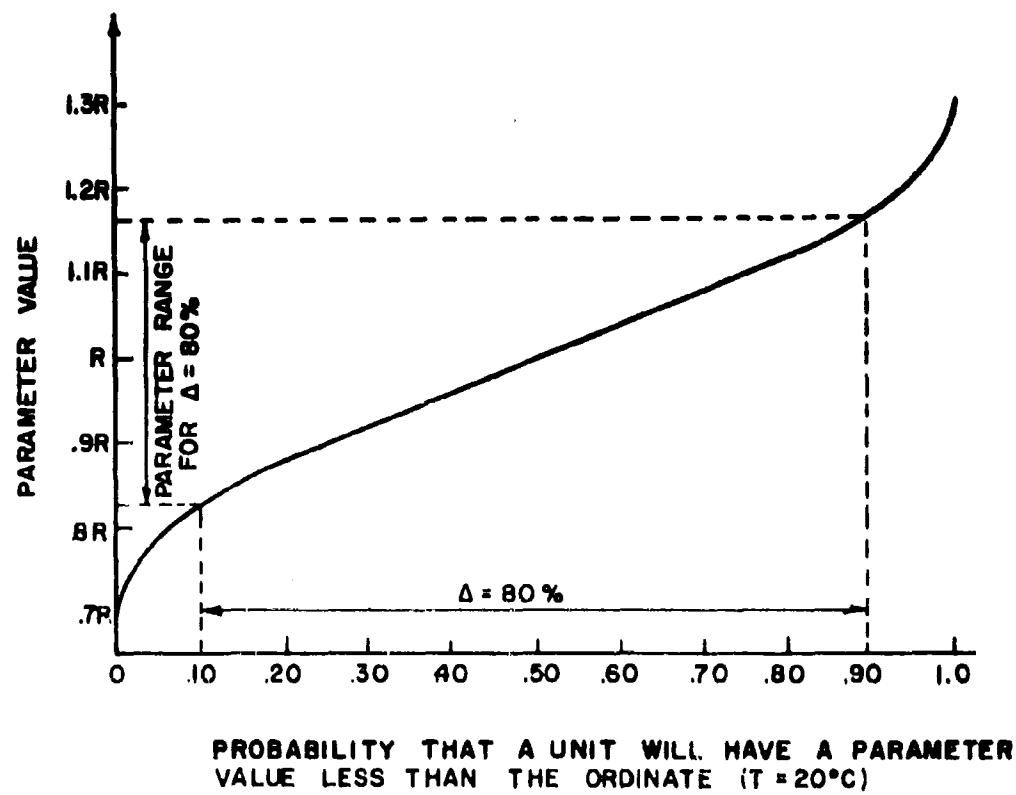


Figure 1. Probability Density, Probability Distribution, and Δ

between 0.83 R and 1.17 R are called the 80% Confidence Interval Values. The degree of confidence, Δ, for the interval 0.83 R to 1.17 R is 80%.

In many physical components, the parameter values are appreciably affected by temperature. Therefore, a multiplicity of probability distribution functions must be considered if more than a single temperature is involved. In Figure 1 the distribution function applies for the components at 20° C. In Figure 2 the distribution function of Figure is repeated along with distribution functions of the same parameter for several other discrete temperatures of the components.

Consider a particular example for the purpose of illustration. The probability distribution of Figure 1 might correspond to a particular brand of "1000 ohm" resistors having a median value of 1000 ohms at 20° C. Figure 13 shows that the median value of the same "1000 ohms" resistors is about 900 ohms at 0° C and 1500 ohms at 80° C. Also, the 80% confidence limits are 830 and 1170 ohms at 20° C but 1220 and 1580 ohms at 80° C.

b. The Degree of Parameter Confidence and its Effect on Reliability

The degree of parameter confidence, Δ, has been defined in the previous section. The greater the magnitude of Δ, the greater is the probability that the parameter values will be within the related confidence limits.

There are circuit design techniques which yield circuits which will always work provided that each parameter is greater than some minimum design value but less than some maximum design value. Let us consider the hypothetical application of one of these design techniques to a circuit which is to operate at a particular temperature. Let us consider that for the minimum and maximum values of each parameter to be used in the design technique, we select the 85% confidence limits (associated with the minimum length confidence interval). The resultant design will have a particular probability of successful operation.

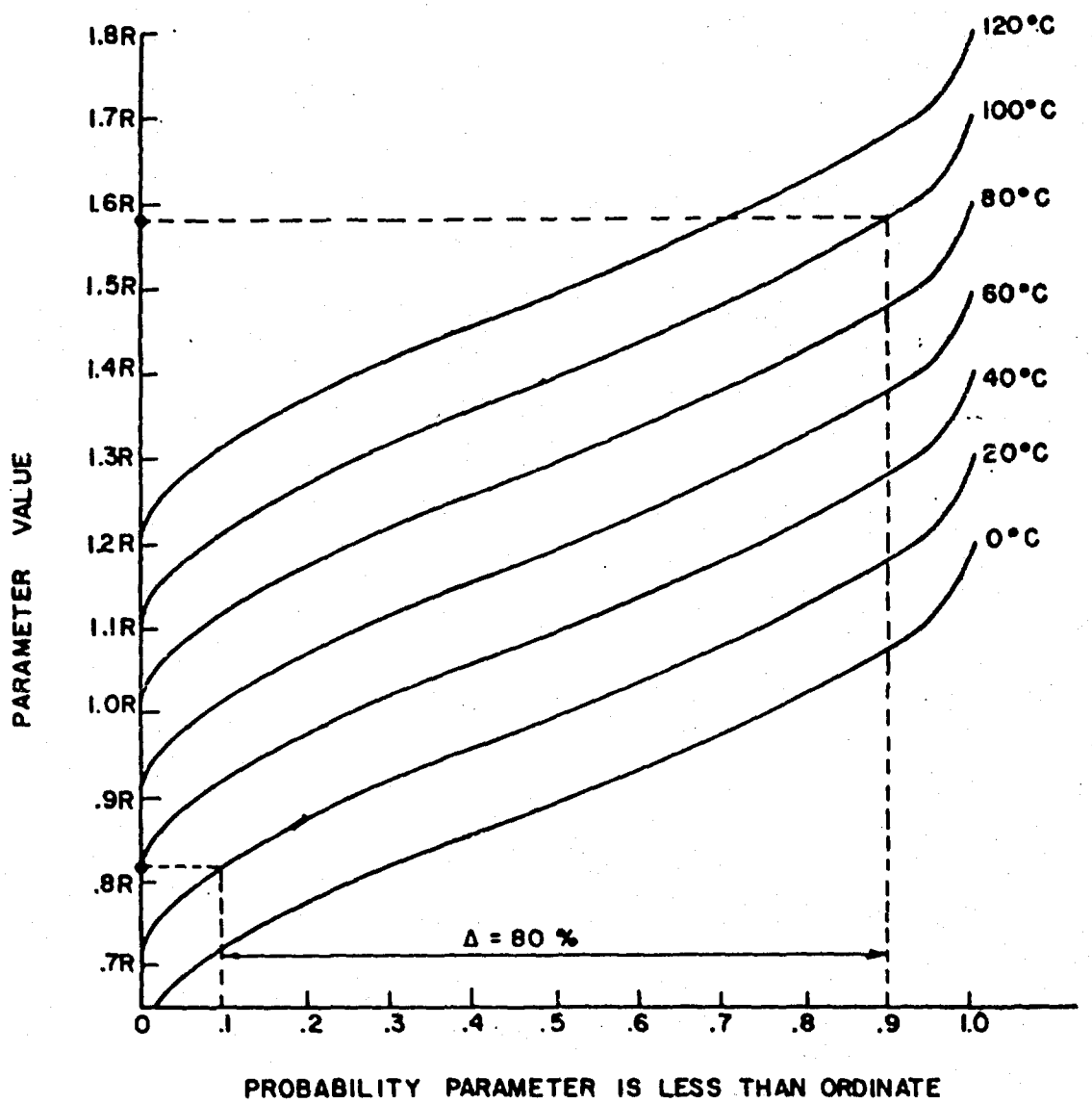


Figure 2. Probability Distribution and Temperature

If we were next to redesign using 95% confidence limits, the resultant circuit would have a higher probability of successful operation than the 85% design. A system composed of the 95% confidence limit circuits would be expected to have a higher probability of successful operation than a system using the 85% confidence designs.

Figure 3 illustrates this idea that the probability of successful system operation is an ever increasing function of the degree of confidence that the individual component parameters are within their design limits. This is an extremely powerful statement. It forms the basis for the Parameter Confidence Design Method outlined in the next section.

2. Design Procedure

The design procedure consists of three relatively independent steps: mapping the circuit realizability plane; establishing the thermal characteristic of the mechanical packaging system; and combining the results of the first two steps such as to find the optimum current design for the given system.

a. Mapping the Realizability Plane

Each realizable plane applies to specific fan-in-fan-out and maximum frequency of operation requirements. Although the realizability plane may represent an infinite number of possible circuit designs, it is mapped by using a relatively small arbitrary number of designs. The realizability plane is generated as a result of answering the questions: for an arbitrary temperature range of operation, is it possible to design a circuit with an arbitrary parameter confidence level? If the design is possible, what is the minimum average power dissipated by such a circuit?

If these questions are answered for an arbitrary number of incremental values of confidence level between 0% and 100% and for an arbitrary number of temperature ranges between the minimum expected ambient temperature of the system and the "melting point" of the components, then all of the realizability plane would be mapped.

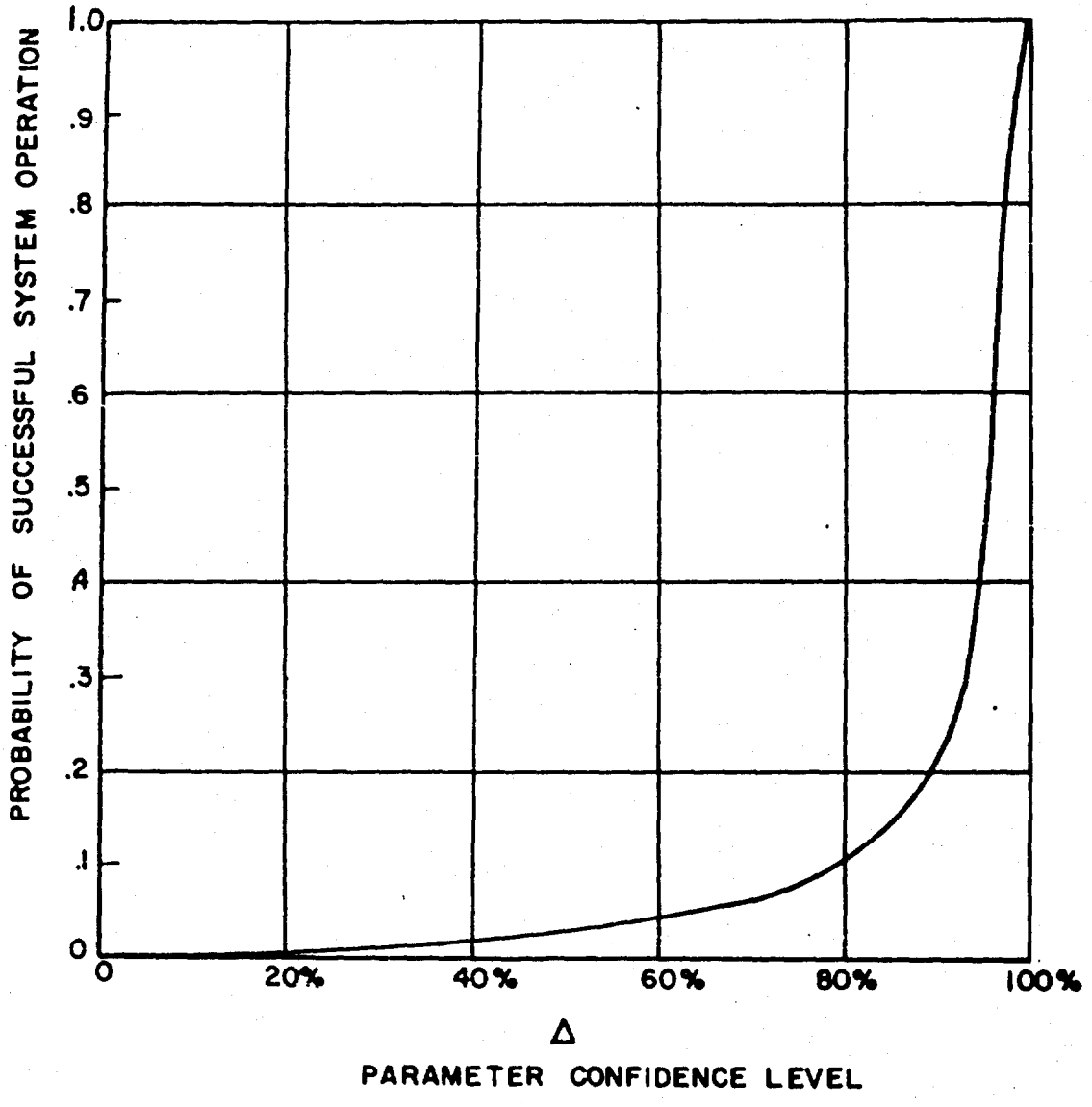


Figure 3. Probability of Success Increases with Parameter Confidence Level

Figure 4 shows the result of a hypothetical mapping. For the present discussion, the dashed lines labeled A,B,C, and D along with the points labeled a,b,c, and d should be ignored. The points on the curves marked with an X indicate the answers to the questions: For the given temperature range of operation and the given degree of confidence what is the minimum average power?

Let us consider in more detail how one of the X designs of Figure 4 was carried out. As a typical example, consider the design for a maximum temperature of 100°C, a system ambient temperature of 20°C and Δ = 80%. The design method requires families of probability distributions, of type shown in Figure 2, for each of the relevant design parameters. The parameter design values are determined using the respective families of probability distributions. The upper design parameter value is selected to be the upper 80% confidence limit on the 100°C distribution. The lower design parameter value is selected to be the lower 80% confidence limit on the 20°C distribution. These choices are made because the resultant design may be expected to operate correctly anywhere between 20°C and 80°C. A minimum power circuit design is carried out using the above upper and lower values for each design parameter. Such a circuit design will dissipate a distribution of possible power magnitudes. The average power dissipated by the particular circuit design was recorded in Figure 4 at the 100°C maximum temperature.

Other designs were carried out in a similar manner for other maximum temperatures of 20°C, 40°C, 60°C, 80°C and 120°C while maintaining the same system ambient temperature of 20°C and confidence level of 80%. The average power was recorded at each of these maximum temperatures. Thus, the curve labeled Δ = 80% was determined.

The procedure was then repeated for the different values of 0%, 98%, 99.9%, 99.95% and 99.99% for Δ.

The result of the whole procedure constituted the mapping of a realizability plane. This realizability plane applies to a fixed fan-in-fan-out and maximum frequency of operation of a particular circuit topology.

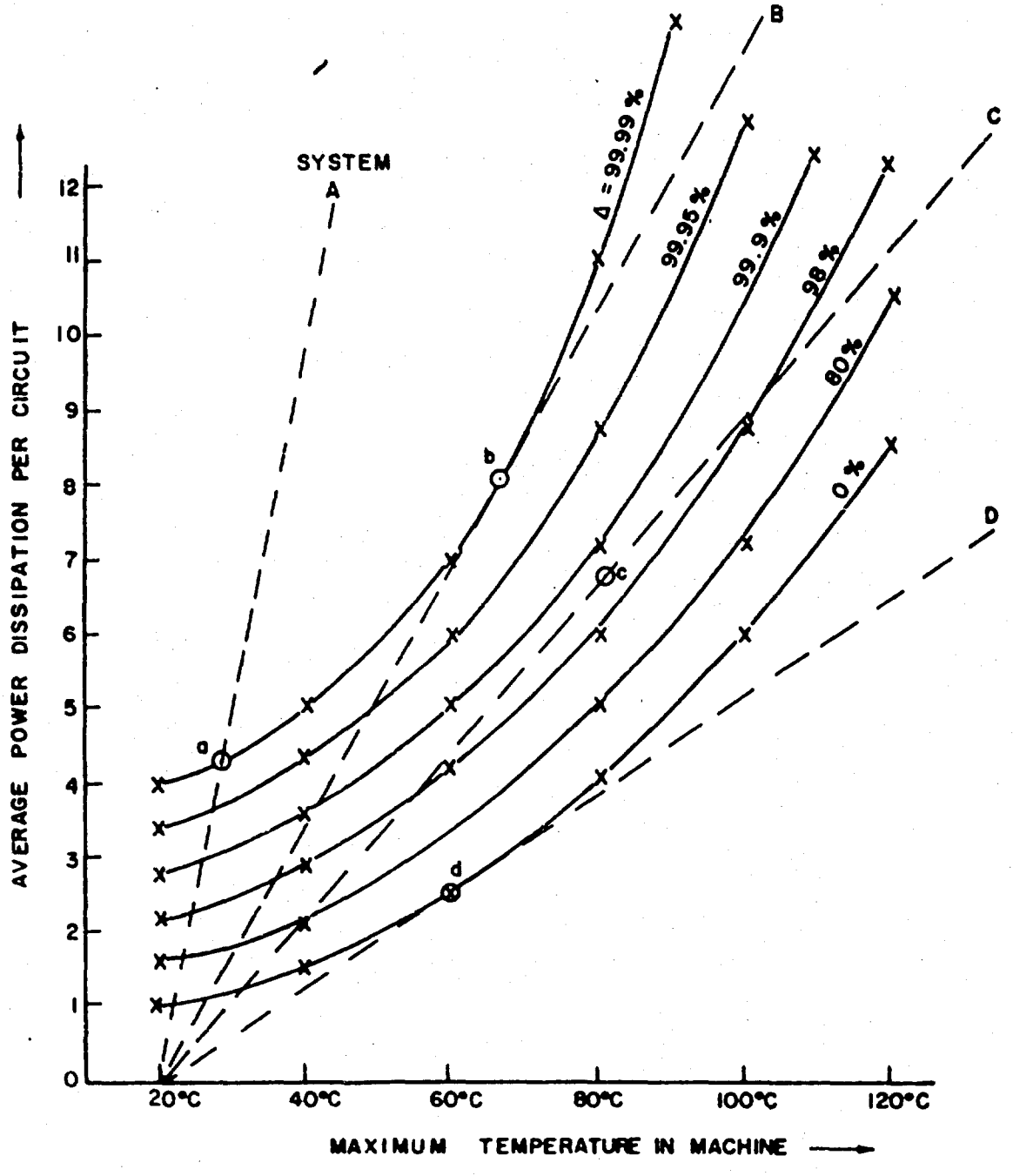


Figure 4. Typical Realizability Plane with Superimposed System Characteristics

It should be emphasized that there is a continuum of possible designs represented by the plane. Each circuit design represents the minimum power design within the constraints of temperature range and parameter confidence level.

b. Thermal Characteristics of Packaging System

A digital machine is composed of a large number of circuit building blocks imbedded in some mechanical packaging system. An essential function of the packaging system, especially in microelectronics, is the removal of the heat generated by the individual circuits.

For any particular type of packaging system, the maximum temperature within the system increases as the power being dissipated by each circuit increases. A graphical presentation of the variation of the maximum temperature within the system with per circuit power dissipation shall be referred to as the "system thermal characteristic". It is important to note that the system thermal characteristic can be generated simply on the basis of a distributed heat source thermal problem. It is only a function of heat conductivities, system geometry, number of distributed heat sources, and the perfectness of the heat sink.

Assuming a perfect heat sink, the maximum temperature within a system will generally increase linearly with per circuit power dissipation. A non-perfect heat sink will in general cause the maximum system temperature to increase in some exponential-type fashion with increasing circuit dissipation.

In either case, the system thermal characteristic can be directly applied in order to find the optimum design as shall be described in the next section.

c. Combining System Thermal Characteristic with a Realizability Plane.

In Figure 4, the dashed lines are the thermal characteristics of four different mechanical systems, labelled A, B, C, and D, all in the same external ambient temperature (namely 20° C). The systems shown are all linear, i.e. the maximum system temperature varies linearly with per circuit power dissipation. However, non-linear system thermal characteristics would be used similarly. System A represents a very effective thermal packaging system wherein appreciable change in per circuit dissipation causes relatively small changes in the maximum temperature in the system. System B is not quite as effective as system A, and system C is not as good as system B. System D is the most inferior of the four in that there is appreciable temperature rise for the same changes in circuit dissipation.

The intersection between the system thermal characteristic and the realizability plane represents the circuits which have been specifically designed for the temperature range of the given system. Any circuit designs that are chosen that do not lie on the intersection can not be better and in general will be extremely less optimum.

Figure 5 shows the value of the degree of parameter confidence, Δ, as a function of maximum temperature for each of the four systems. These curves were directly derived from the intersections of Figure 4.

Based on the ideas illustrated in Figure 3 we would select, for each system, the design for which the degree of parameter confidence is highest. The maximum Δ designs are indicated by points a, b, c, and d in Figure 4.

It should be noted that there is a tremendous difference between knowing something to 99% to 99.9% confidence when one is considering large numbers of simultaneous occurrences. Figure 6 illustrates the effect of large numbers.

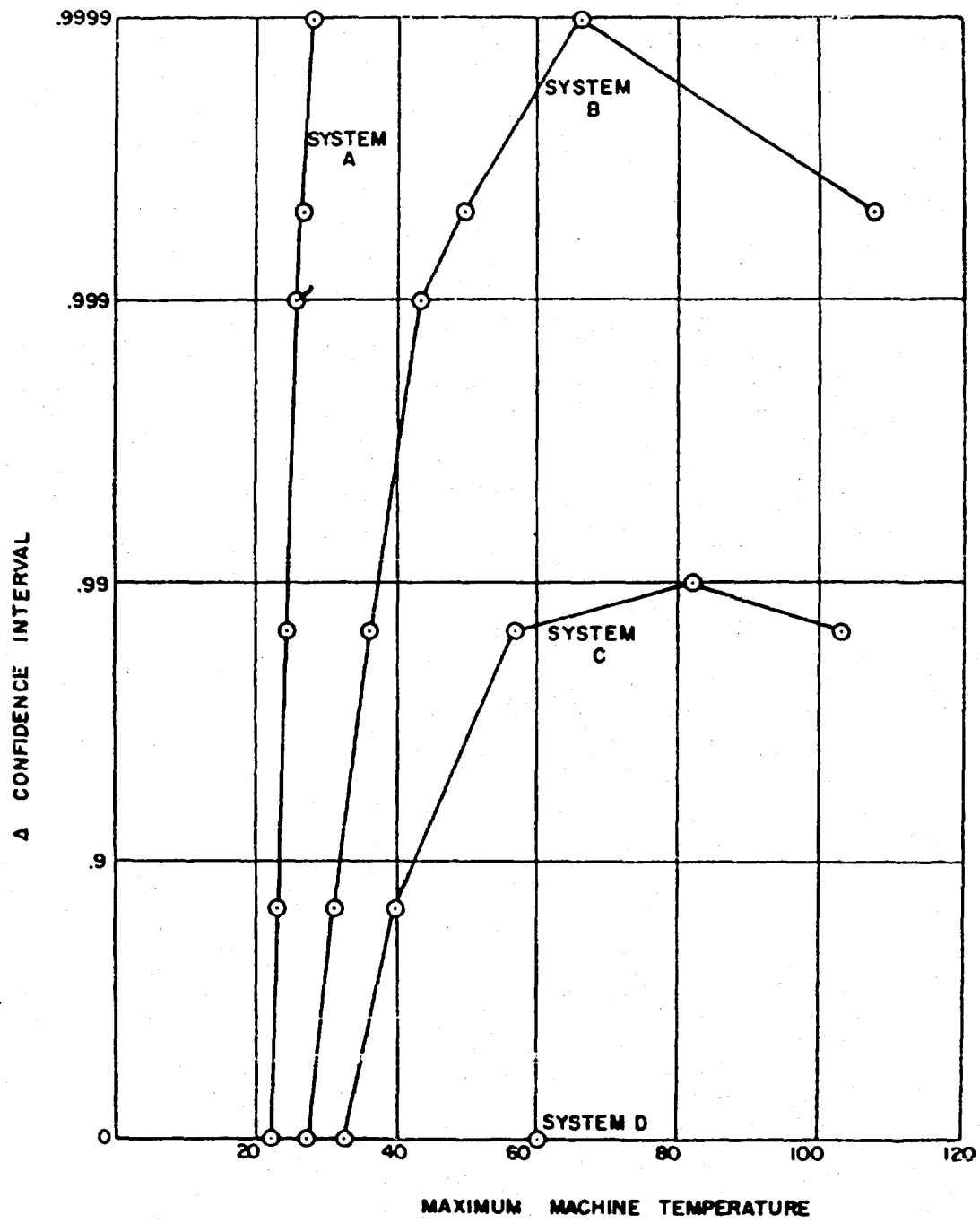


Figure 5. Design Confidence Interval vs. Temperature For Given Systems

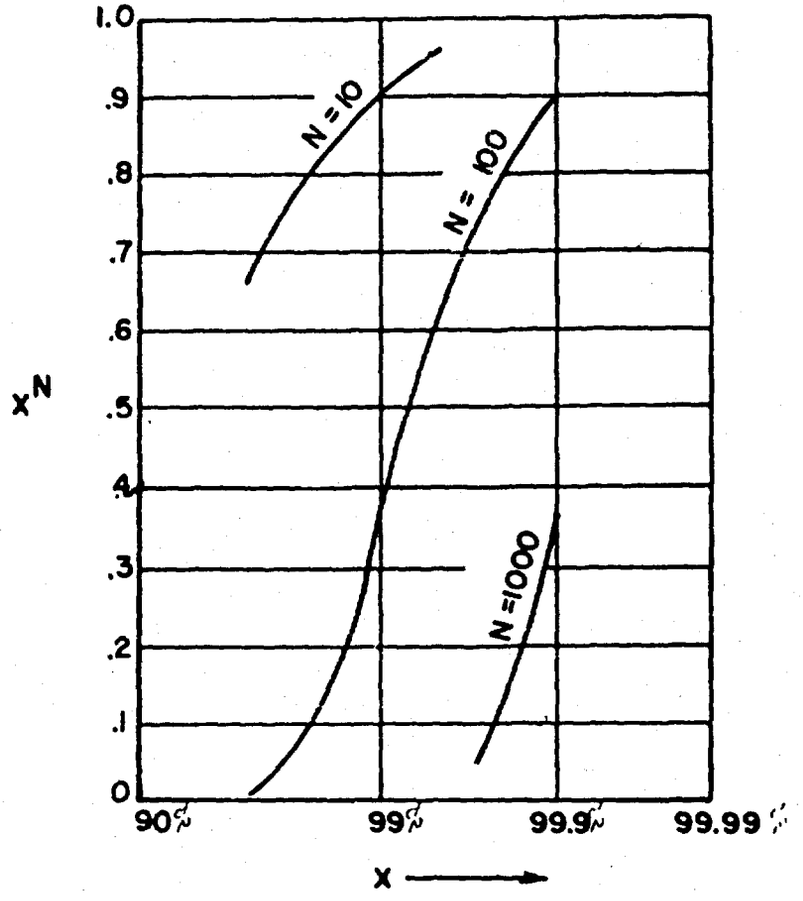


Figure 6. Effect of Number on the Cumulative Probability of Success

3. Some Conclusions and Observations

This parameter confidence design method is new and as yet unproved. It seems to be very powerful in the sense that the graphical approach allows one to work with extremely skewed and elongated parameter distributions as simply as one does with truncated or rectangular distributions. Also, the graphical solution seems to allow much visualization as to the effect of perturbations in parameters and thermal systems.

A very striking possibility indicated by this method is that there exists a distinct optimum design for a particular system which is independent and exclusive of catastrophic failure!

This method allows catastrophic failures to be handled as "bumps" on the tails of the parameter probability density functions, thus eliminating the necessity of attempting to differentiate between extreme "drift" failures and catastrophic failures.

If components are to be selected such as to cause the probability of drift failure to approach zero, the parameter Confidence Method indicates the design which will give maximum component yield.

In situations where components cannot be selected out (e.g., unified thin film subsystems; multi-element functional blocks; etc.) parameters will in general be distributed in some non-truncated distribution (e.g Gaussian). This method can be applied to truncated or non-truncated distributions with equal simplicity. In this case, the circuit design with the least probability of failure can be determined.

The Parameter Confidence Design Method explicitly emphasizes the effect of system thermal characteristics on the realizability and design of the maximum reliability circuit for any arbitrary system. In cases where it is impractical to select components, it can be ascertained as to what degree the system thermal characteristics must be changed to sufficiently decrease the probability of failure.

Needless to say, much elaborate parameter distribution data is necessary before this method can be effectively implemented. Unfortunately, this is not available at this time. Since many of the conclusions are a direct result of the actual numbers involved, hypothetical or assumed data does not particularly prove anything.

APPENDIX C-1

Terminal Parameter Measurements

The method of Terminal Parameter Measurements has been adopted to determine circuit parameter values and to analyze the performance of a microelectronics fabricated circuit. By means of the measurement results the circuit design equations, and the design specifications, the performance of the circuit can be predicted. This is also a method of checking the fabrication techniques.

Two general circuit blocks, a general transistor amplifier, and a general transistor flip-flop are the cases in point. For the passive components, accuracy is limited only by instrument accuracy. For the active devices, only ball park figures are meaningful, and measurements showed that device parameters are measureable to ball park accuracy.

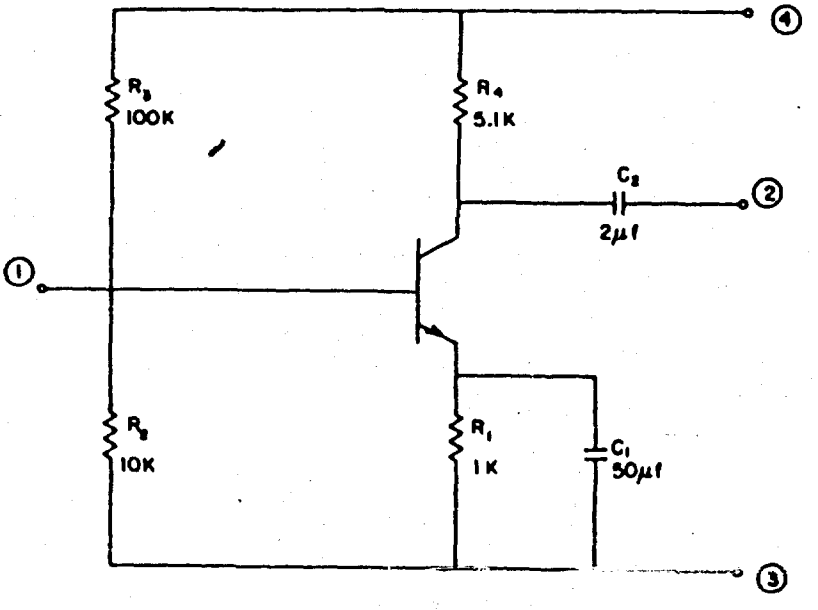


Figure 1. Amplifier with Four Available Terminals; Component values as Indicated.

For the experimental measurements a circuit with the component values indicated in Figure 1 was used. A convenient approach to the amplifier is to consider the transistor as two back-to-back diodes. There will then be three separate sets of measurements in the analysis. First, consider those components associated with the collector-base diode. In this case utilize terminals (1), (2), (4) in Figure 2 and leave terminal (3) open. Second, consider those components connected to the emitter-base diode utilizing terminals (1), (3) and leaving terminals (2), (4) open. Finally, consider the transistor as a single device and evaluate some of its important parameters.

a. Collector - Base Diode Network

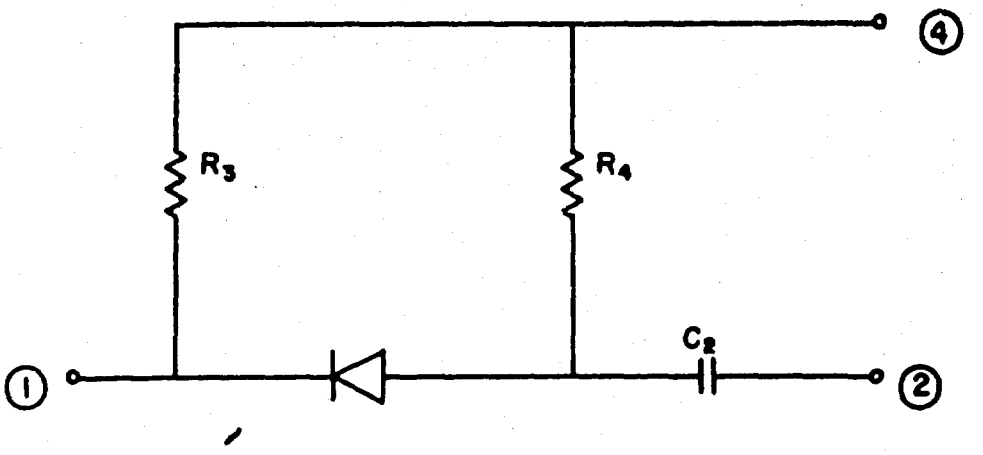


Figure 2. Equivalent Circuit with Terminal Left Open.

(1) Determination of R_3

The approach is dependent upon whether the transistor is germanium or silicon. The procedure is based on biasing the diode in its non-conducting region. For a silicon transistor (e.g., 2N706) this is accomplished by a DC measurement of the voltage between terminals (1) - (4) and the current into one of the terminals. This measurement yields R_3 = 98 K.

If the transistor is germanium (e.g. 2N396), there is an additional problem due to leakage current of approximately 10μa in its back-biased state. This current is approximately constant with voltage.

Since R_3 is quite large, this leakage introduces error into the measurement. The measurement, however, is achieved by an AC voltage-current measurement with the diode back-biased, since the current through the diode is constant. This measurement yields R_3 = 100 K.

(2) Determination of R_4

Both germanium and silicon diodes are low resistance devices when they are forward biased. However, their DC resistance is not so small as to be negligible, especially in silicon, which has a conduction threshold of approximately 0.7 volt. The incremental resistance is sufficiently low, however, to be neglected for an AC measurement. An AC measurement with the diode of Figure forward biased then yields the parallel resistance of R_3 and R_4. Solving the resulting expression for R_4, the result is R_4 = 5.0K.

(3) Determination of C_2

This measurement can be accomplished using an admittance bridge across terminals (2) - (4). Also bias between

terminals (1) - (4) in order to back bias the collector-base junction. The admittance between terminals (2) - (4) is given by

$$Y = G + jB = \frac{1}{R_4} \frac{\omega^2 C_2^2 R_4^2}{1 + \omega^2 C_2^2 R_4^2} + j\omega C_2 \frac{1}{1 + \omega^2 C_2^2 R_4^2} \quad (1)$$

Equating the real parts in order to solve for C_2, results in

$$C_2 = \frac{1}{2\pi f} \frac{G}{R_4 (1 - R_4 G)} \quad (2)$$

R_4 is known and G is the real component of the measured admittance. Since C_2 is a large capacitor, the measurement is made at low frequency. At 20 cps the balanced bridge reads

$$Y = 120\ \mu\text{ mho} + j\ 450\ \mu\text{ mho}$$

Using the value G = 120 μ mho in Equation (2)

$$C_2 = 1.94\ \mu\text{f}$$

b. Emitter - Base Diode Network

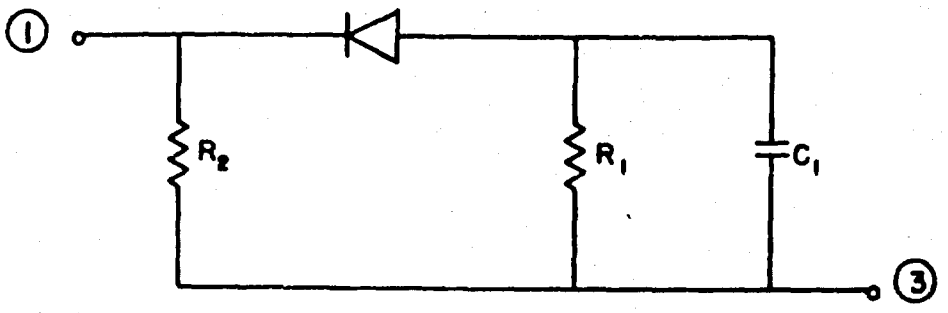


Figure 3. Equivalent Amplifier Circuit with Terminals (2), (4) Open.

(1) Determination of R_2

The procedure is identical to the determination of R_3 in the collector-base diode circuit. This measurement gives $R_2 = 10$ K.

(2) Determination of R_1

The presence of the bypass capacitor C_1 prevents a simple AC measurement of the type employed in the evaluation of R_4 in the collector-base diode circuit. However, the difference between two DC measurements will serve the purpose of an incremental measurement. Two separate measurements then will lead to

$$\frac{R_1 R_2}{R_1 + R_2} = \frac{\Delta v}{\Delta i} \qquad (3)$$

This results in a value of $R_1 = 1$ K.

(3) Determination of C_1

The value of C_1 can be obtained by means of an impedance measurement between terminals (1) - (3). Forward bias the diode by a voltage source in series with a large resistance. The large resistance is used so as not to affect the measurement. The parallel impedance of the bypass capacitor and emitter resistor is quite low, as is the incremental diode impedance. Thus, neglect the impedance of R_2 in parallel with them. The impedance between terminals (1) - (3) will then be

$$Z = R + jX = r_{DE} + R_1 \left[\frac{1}{1 + \omega^2 R_1^2 C_1^2}\right] + \frac{1}{j\omega C_1}\left[\frac{1}{1 + \frac{1}{\omega^2 R_1^2 C_1^2}}\right] \qquad (4)$$

where r_{DE} is the incremental diode impedance. Even at low frequencies C_1 is of such great magnitude that $\omega^2 R_1^2 C_1^2 >> 1$.

This approximation simplifies the impedance expression so that Equation (4) becomes

$$Z = r_{DE} + \frac{R_1}{\omega^2 R_1^2 C_1^2} + \frac{1}{j\omega C_1} \qquad (5)$$

The bridge balances for

$$Z = 60\Omega + \frac{1}{j}\ 30\Omega$$

This leads to the value of $C_1 = 53\ \mu f$.

c. Important Transistor Parameters

The following data are for the 2N188A audio frequency transistor. Because of transistor variations it is only possible to obtain ball park results for the following parameters.

(1) Determination of β and the Common Emitter Cutoff Frequency

β_o is the common emitter short circuit current gain. Apply the design voltage between terminals (3) - (4) in order to achieve normal circuit operation. Tie together (2) - (3) through a 100Ω resistor to approximate an AC short circuit at the output. Drive the circuit between terminals (1) - (3) with an AC generator in series with a 100 K resistor to approximate a small signal current source. β_o is then given by

$$\beta_o = \frac{i_c}{i_b} = \frac{v_{2/100\Omega}}{v_1/100\ K} \qquad (6)$$

At 100 cps and a one-volt input the measurement yields $\beta_o = 45$. This is the low frequency gain or β_o. Increase the frequency to find the common emitter cutoff frequency ω_β, which is that frequency for which

$$\beta = \frac{\beta_o}{\sqrt{2}} \qquad (7)$$

The cutoff frequency is found to be

$$\omega_\beta = 314\ KC.$$

The common base cutoff frequency is related to the common emitter cutoff frequency by Equation (8).

$$\omega_\alpha = \frac{\omega_\beta}{1 - \alpha} = \omega_\beta (1 + \beta) \qquad (8)$$

This gives for the common base cutoff frequency

$$\omega_\alpha = 14.4 \text{ mc}$$

(2) Determination of Collector Admittance

Measure directly between terminals (1) - (2) leaving the others open. This admittance will include both leakage and diffusion parameters. Measurement on the bridge gives

$$Y = \frac{1}{6.0 \text{ K}} + j\omega \ 162 \text{ pf}$$

(3) Emitter Diffusion Resistance

At low frequencies r_ϵ is approximately the common base input impedance with the output short circuited. Short terminals (1) - (2) and measure the impedance between (1) - (3). Make ω just large enough so that the impedance of C_2 will be no more than about 100 Ω. This is true for a frequency of about 1 kc. This is still sufficiently low that the emitter diffusion capacitance will have no effect. The measurement gives

$$r_\epsilon = 1.4 \text{ K}$$

The capacitance can be obtained using the relation

$$r_\epsilon C_\epsilon \approx \omega_\alpha \qquad (9)$$

which yields

$$C_\epsilon \approx 50 \text{ pf}$$

(4) Base Spreading Resistance

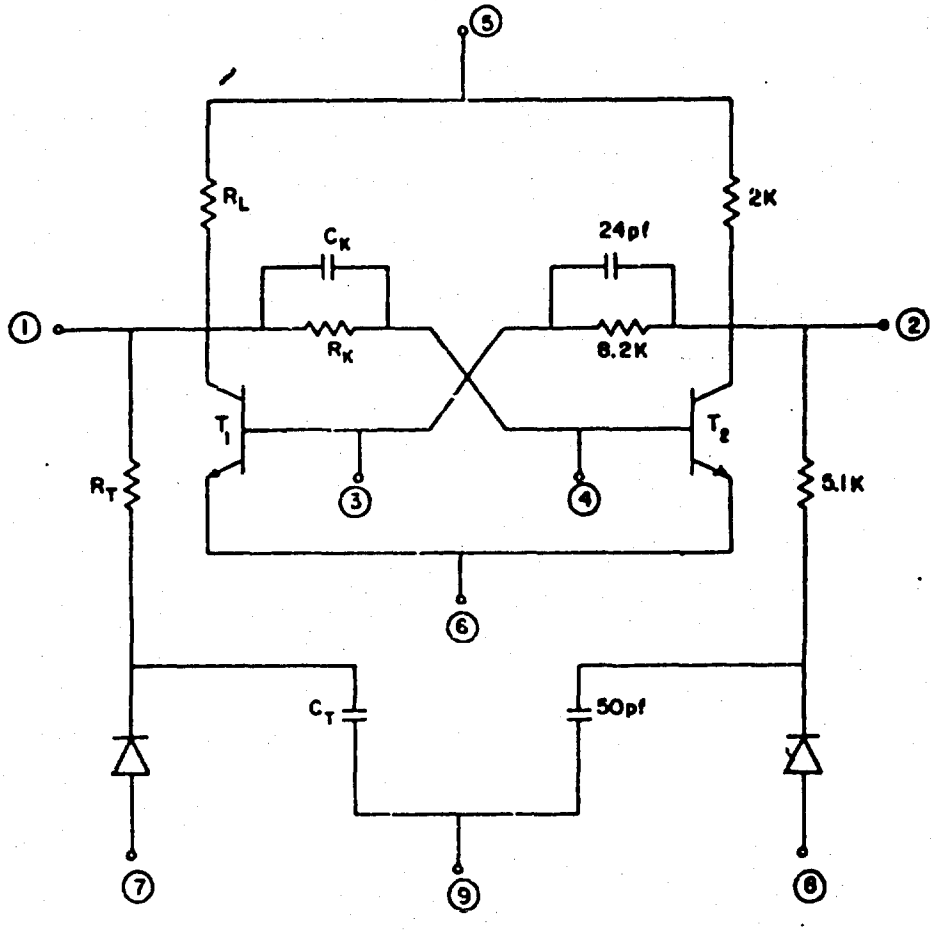
At high frequencies, the input impedance between terminals (1) - (3) with (2) - (3) shorted is approximately r_b'. At a frequency of 15 mc, the bridge measures

$$Y = \frac{1}{47\Omega} + j(\sim 0)$$

The base spreading resistance is then

$$r_b' \approx 47\Omega.$$

2. Flip-Flop Circuit



THE TRANSISTORS ARE 2N706
THE TRIGGER DIODES ARE HD2569

Figure 4. Flip-flop with Nine Available Terminals; Component Values as Indicated.

a. Passive Circuit Components

(1) Determination of R_L

Ground terminal (6) and connect terminal (5) to a positive voltage source, in this case a three-volt source. Measure the current into terminal (5) and compute R_L from Equation (10).

$$R_L = \frac{2V_s - V_{c_1} - V_{c_2}}{I_s} \qquad (10)$$

V_{c_1} is the voltage at terminal (1).

V_{c_2} is the voltage at terminal (2).

V_s is the source voltage.

I_s is the source current.

This leads to the value $R_L = 1.94$ K.

(2) Determination of R_k

Apply a DC voltage between terminals (2) - (3) with terminal (2) positive to prevent the transistors from conducting. Measure the current into terminal (2) to obtain R_k directly. The measured value is $R_k = 8.2$ k.

(3) Determination of R_T

Make an AC measurement of the voltage and current between terminals (1) - (7) with the trigger diode forward biased. Leave the other terminals open. This yields for R_T

$$R_T = 5.1 \text{ K}$$

(4) Determination of C_T

Make an admittance measurement between terminals (1) - (9) with the other terminals open. The admittance expression is then

$$Y = G + j B = 2 \left[\frac{1}{R} \frac{1}{1 + \frac{1}{\omega^2 R^2 C_T^2}} + j\omega C_T \frac{1}{1 + \omega^2 R^2 C_T^2} \right] \qquad (11)$$

where $R = R_T + R_L$.

Equate the real parts of Equation (11) to obtain an expression for C_T

$$C_T = \frac{1}{2\pi f} \left[- \frac{\frac{1}{2} G}{R \left(1 - R \frac{G}{2}\right)} \right]^{\frac{1}{2}} \qquad (12)$$

The bridge balances for

$$Y = \frac{1}{6.4\ K} + j\omega\ 45\ \text{pf}.$$

Substituting $G = \frac{1}{6.4\ K}$ into Equation (12) leads to $C_T = 50$ pf.

(5) Determination of C_k and C_E

Two measurements are necessary to evaluate C_k due to difficulty in isolating it from transistor emitter capacitance. The measurements lead also to the evaluation of the emitter-base junction capacity, C_E, of the transistor.

To find C_E tie together terminals (3) - (4) and measure the admittance between terminals (3) - (6). Let the other terminals remain open and use no DC bias; i.e., measure the emitter capacity at a DC operating point of zero voltage and current. The admittance is then given by

$$Y = 2\ j\omega\ C_E \tag{13}$$

The bridge balances at

$$Y = j\omega\ 24\ \text{pf}$$

This means that at zero bias

$$C_E = 12\ \text{pf}.$$

Now make another admittance measurement, this time between terminals (1) - (2). Fix the other terminals as follows:

Short together (1) - (3)
Short together (2) - (4) - (5) - (9)
Leave open (6) - (7) - (8)

At zero bias the emitter-base junction will not conduct so the diode model is essentially just a capacitor of value C_E.

The equivalent circuit between terminals (1) - (2) is shown in Figure 5. The expression for the admittance is given by Equation (14).

$$Y = \frac{1}{R_L} + 2\ \frac{1}{R_k} + \frac{1}{R_T}\left[\frac{1}{1 + \omega^2 R_T^2 C_T^2}\right] \tag{14}$$

$$+ j\omega\left[2\ C_k + \frac{1}{2}\ C_E + C_T\ \frac{1}{1 + \omega^2 R_T^2 C_T^2}\right]$$

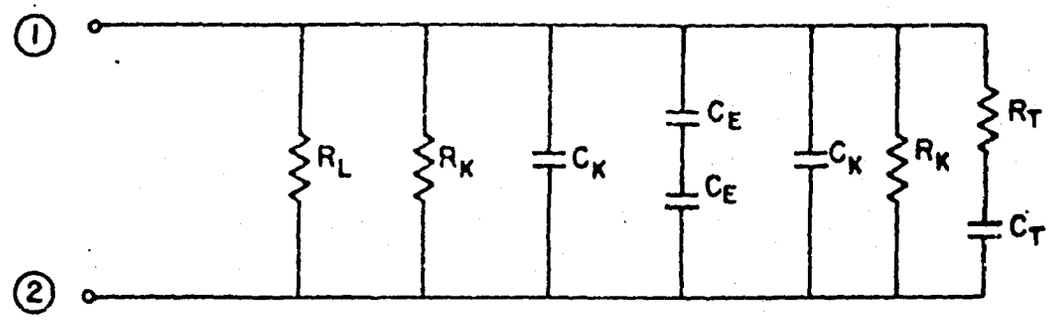


Figure 5. Equivalent Admittance for Measurement of C_k.

Equate the imaginary parts of Equation (15) and solve for C_k.

$$C_k = \frac{1}{2}\left[\frac{B}{\omega} - \frac{1}{2} C_E - C_T \frac{1}{1 + \omega^2 R_T^2 C_T^2}\right] \qquad (15)$$

where $B = \text{Im}\left[Y\right]$.

The frequency of measurement is 500 kc and the bridge balances at

$$\overline{Y} = \frac{1}{1.8\ K} + j\omega\ 86\ pf$$

Solving Equation (15) with $B = \omega$ 86 pf gives C_k = 25 pf.

b. Transistor Parameters

(1) Determination of Collector Capacity

In solving for C_k, the emitter capacity was also computed. Now make an admittance measurement to obtain C_c, the collector capacity, set up the circuit as follows:

Short out terminals (1) - (2)

Ground terminals (3) - (4)

Supply the design voltage at terminal (5) to obtain normal operation.

Let terminals (6) - (7) - (8) remain open.

The collector-base junction is here back biased at 2.15 volt so that the diode model is just C_c.

The equivalent circuit is shown in Figure 6.

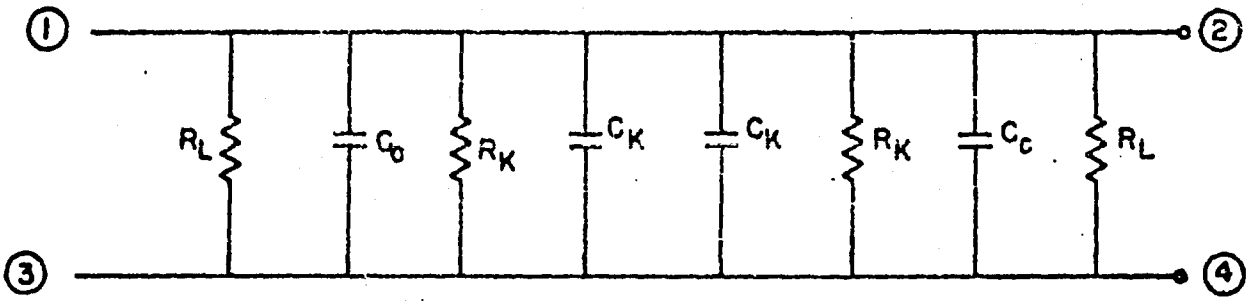


Figure 6. Equivalent Circuit for Measurement of C_c.

An admittance measurement between terminals (1) - (3) will then give an expression for C_c. The admittance between (1) - (3) is

$$Y = 2 \left[\frac{1}{R_L} + \frac{1}{R_k} + j\omega (C_k + C_c) \right] \tag{16}$$

Equate the susceptive components and solve for C_c

$$C_c = \frac{1}{2} \frac{B}{\omega} - C_k \tag{17}$$

The bridge balances for

$$Y = \frac{1}{740\Omega} + j\omega (74 \text{ pf}) = G + j B$$

This gives for C_c at 2.15 v bias C_c = 12 pf.

(2) Gain-Bandwidth Product and Minority Carrier Storage Factor

For this measurement set up the flip-flop for normal operation:

Ground Terminal (6)
Apply design voltage to (5)

Tie together terminals (3) - (7)

Tie together terminals (4) - (8)

Connect square wave trigger between terminal (9) and ground

Leave terminals (1) - (2) open

This permits measurement of the trigger charge, Q_T. It consists of a saturation charge, Q_s, which is necessary to pull the conducting transistor out of saturation and a regenerative charge, Q_r, which drives it from the edge of saturation to the cutoff condition, thus switching the flip-flop from one state to the other. Equations (18), (19), and (20) define Q_T, Q_R and Q_S.

$$Q_T = Q_R + Q_S \tag{18}*$$

$$Q_R = \frac{I_{ca}}{\beta_{\alpha\beta}} + \Delta V_c C_c \tag{19}$$

$$Q_S = K_S \left[I_B - \frac{I_c}{\beta} \right] \tag{20}$$

where

I_{ca} = collector current at edge of saturation

I_c = collector current in saturation region

I_B = base current in transistor

ΔV_c = collector voltage swing.

(3) Determination of Voltages, Currents and Beta Gain

The collector current in the saturation region is

$$I_c = \frac{V_s - V_{CES}}{R_L} \tag{21}$$

and at the edge of saturation is

$$I_{ca} = \frac{V_s - V_{CE}}{R_L} \tag{22}$$

where V_{CE} in the latter equation is equal to V_{BE}.

---

*V.P. Mathis, J.J. Suran, "Comparative Performance of Saturating and Current Clamped Pulse Circuits", Internal General Electric Company Report.

The base current in the conducting transistor is

$$I_{B_1} = \frac{V_s - V_b}{R_L + R_K} \tag{23}$$

where V_b is the voltage at the base terminal of the conducting transistor.

β is the current gain which can be computed by means of the circuit of Figure 7.

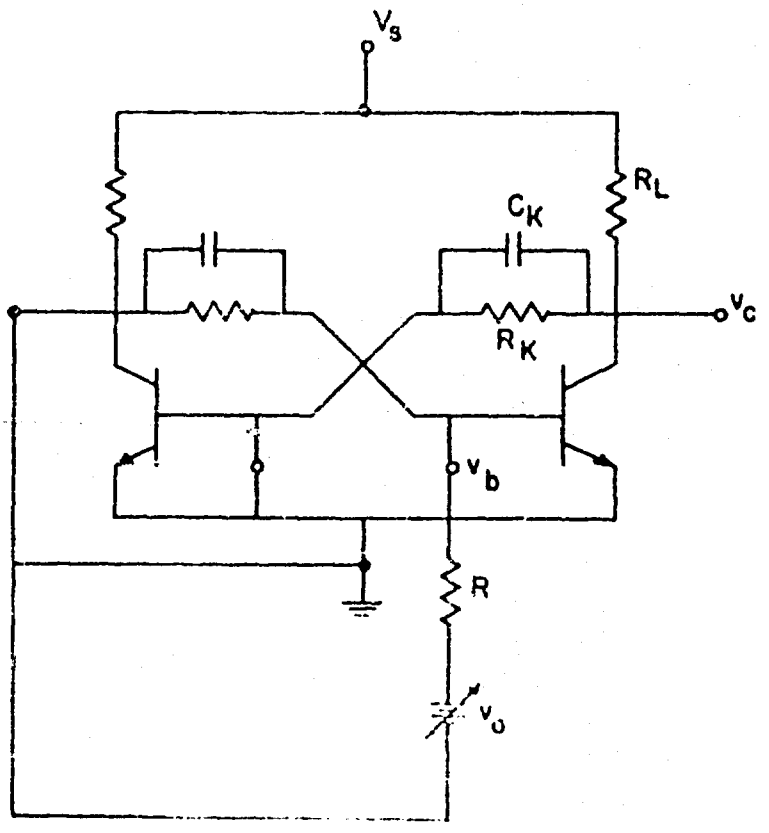


Figure 7. Circuit for Measuring β

Here terminals (7) - (8) - (9) are left open. Because of the leakage of collector current through R_K, use a higher supply voltage to maintain the collector current in the proper range. Compute β by the following equations,

$$\beta = \frac{\Delta I_c}{\Delta I_b} \tag{24}$$

$$I_c = \frac{V_s - V_{CE}}{R_L} - \frac{V_{CE}}{R_K} \tag{25}$$

$$I_B = \frac{V_o - V_{BE}}{R} - \frac{V_{BE}}{R_K} \tag{26}$$

Over the linear region of the transistor

$$\beta = 34$$

(4) Determination of Q_c and Q_s

The approach is to determine Q_R and Q_s by making two measurements and solving the simultaneous equations

$$Q_{T_1} = Q_R + K_s \left[I_{B_1} - \frac{I_{C_1}}{\beta} \right] \tag{27}$$

$$Q_{T_2} = Q_R + K_s \left[I_{B_2} - \frac{I_{C_2}}{\beta} \right] \tag{28}$$

where I_{B_1} is given by Equation (23), I_{C_1} and I_{C_2} are given by Equation (21), β is previously determined and I_{B_2} is yet to be defined. The measurements are:

(a) Measure the minimum trigger charge for the normally operating flip-flop. This is

$$Q_{T_1} = C_T V_{T_1} \tag{29}$$

where V_{T_1} is the minimum square wave amplitude to trigger the flip-flop.

(b) Measure Q_{T_2} with the flip-flop in a clamped state as indicated in Figure 8.

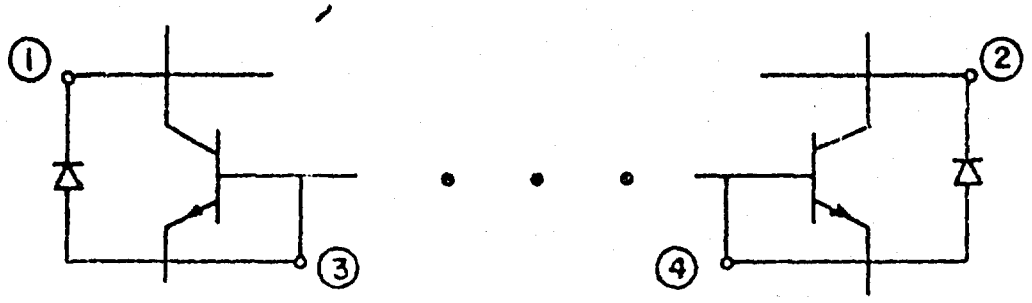


Figure 8. Clamping Diode Connections.

For this configuration the clamping diode partially pulls the conducting transistor out of saturation with the base current, I_{B_2}, defined by

$$I_{B_2} = \frac{V_s - V_b}{R_K + R_L} - I_D \qquad (30)$$

The diode current, I_D, is determined by measuring its voltage drop in the circuit and externally determining the current at this operating point.

Now solve Equations (27) and (28) for Q_R and K_s. The gain bandwidth product is obtained through Equation (19). The results of the measurements are

$$\beta_{\omega\beta} = 156 \text{ mc}$$

$$K_s = 0.22 \ \mu \text{ sec}$$

$$\omega_\beta = 4.6 \text{ mc}$$

Find the common base cutoff frequency, $\omega_{\alpha 1}$ by Equation (31).

$$\omega_\alpha = (\beta + 1)\, \omega_\beta \tag{31}$$

This yields

$$\omega_\alpha = 160 \text{ mc.}$$

DISTRIBUTION LIST

	Copies
Continental Army Command Liaison Office U.S. Army Electronics Research and Development Laboratory Fort Monmouth, New Jersey	3
Commanding Officer U.S. Army Electronics Materiel Support Agency Fort Monmouth, New Jersey Attn: SELMS/ES-ADJ	1
Commanding General U.S. Army Electronics Command Fort Monmouth, New Jersey Attn: AMSEL-CG	1
Commanding Officer, 9560th TSU Signal Corps Electronics Research Unit P. O. Box 205 Mountain View, California	1
Commanding General U.S. Army Electronic Proving Ground Fort Huachuca, Arizona Attn: Technical Library	1
Director, U.S. Naval Research Laboratory Code 2027 Washington 25, D. C.	1
Commanding Officer and Director U.S. Navy Electronics Laboratory San Diego 52, California	1
Commander Wright Air Development Division Wright-Patterson AFB, Ohio Attn: WCOSI-3	2
Commander Air Force Cambridge Research Center L. G. Hanscom Field Bedford, Massachusetts	1
Commander Rome Air Development Center Griffiss Air Force Base, New York Attn: RCSST-3	1

Commander
Armed Services Technical Information Agency
Arlington Hall Station
Arlington 12, Virginia — 10

Advisory Group on Electron Devices
346 Broadway
New York 13, New York — 2

Commanding Officer
Frankford Arsenal
Philadelphia 37, Pennsylvania
Attn: ORDBA-FEL — 1

Commanding General
Redstone Arsenal
Huntsville, Alabama
Attn: Technical Library — 1

Commanding Officer
Watertown Arsenal
Watertown, Massachusetts
Attn: OMRO — 1

Marine Corps Liaison Office
U.S. Army Electronics Research and Development Laboratory
Fort Monmouth, New Jersey — 2

Department of the Navy
Chief, Bureau of Ships
Semiconductor Unit, Code 691A
Washington 25, D. C.
Attn: A. H. Young — 1

Commanding Officer
Diamond Ordnance Fuze Laboratories
Connecticut Avenue and Van Ness Street, N. W.
Washington 25, D. C.
Attn: T. Liimatainen — 1

Chief of Ordnance
Washington 25, D. C.
Attn: ORDTX-AR — 1

Technical Library
OASD (R and E)
Rm. 3E1065, The Pentagon
Washington 25, D. C. — 1

Chief of Research and Development
OCS, Department of the Army
Washington 25, D. C. — 1

Chief, U.S. Army Security Agency
Arlington Hall Station
Arlington 12, Virginia — 2

Deputy President
U.S. Army Security Agency Board
Arlington Hall Station
Arlington 12, Virginia — 1

Motorola, Inc.
1450 No. Circero Avenue
Chicago 51, Illinois — 1

Texas Instruments, Inc.
Semiconductor-Comp Division
13500 No. Central Expressway
Dallas, Texas
Attn: Jack Kilby — 1

Westinghouse Electric Corporation
Air Arm Division
Baltimore, Maryland — 1

Commanding Officer
U.S. Army Electronics Materiel Agency
Fort Monmouth Procurement Office
Fort Monmouth, New Jersey
Attn: Contracting Officer — 1

Motorola, Inc.
Semiconductor Products Division
5005 E. Mc Dowell Road
Phoenix 8, Arizona — 1

Commanding Officer
U.S. Naval Air Development Center
Johnsville, Pennsylvania
Attn: EL-56, Howard Martin — 1

Commander
Aeronautical Systems Division
Wright-Patterson Air Force Base, Ohio
Attn: ASRNEM — 1

Best Available Copy

Commanding Officer
U.S. Army Electronics Research and Development Laboratory
Fort Monmouth, New Jersey

Attn:	Director of Reseach	1
Attn:	Chief, Technical Documents Center	1
Attn:	Chief, Technical Information Division	3
Attn:	Chief, Microwave and Quantum Electronics Br, Solid State and Frequency Control Division	1
Attn:	Reports Distribution Unit, Solid State and Frequency Control Division (Record Copy)	1
Attn:	Director, Solid State and Frequency Control Division	1
Attn:	J. Hohmann, Solid State and Frequency Control Division	37

Best Available Co

UNCLASSIFIED

UNCLASSIFIED